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Development of CdTe Thin Film Solar Cells on Flexible Foil Substrates

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by

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ABSTRACT

Cadmium telluride (CdTe) is a leading thin film photovoltaic (PV) material due to its near ideal band gap of 1.45 eV, its high optical absorption coefficient and availability of various device fabrication methods. Superstrate CdTe solar cells fabricated on glass have to-date exhibited efficiencies of 16.5%. Work on substrate devices has been limited due to difficulties associated with the formation of an ohmic back contact with CdTe. The most promising approach used to-date is based on the use of an interlayer between the CdTe and a metal electrode, an approach that is believed to yield a pseudo-ohmic contact. This research investigates the use of ZnTe and Sb_2Te_3 as the interlayer, in the development of efficient back contacts.

Excellent adhesion and minimum stress are also required of a CdTe thin film solar cell device on a flexible stainless steel (SS) foil substrate. Foil substrate curvature, flaking, delamination and adhesion as a result of compressive strain due to the coefficient of thermal expansion (CTE) mismatch between the flexible SS foil substrate and the solar cell films have been studied. A potential problem with the use of a SS foil as the substrate is the diffusion of iron (Fe), chromium (Cr) and other elemental impurities into the layers of the solar cell device structure during high temperature processing. A diffusion barrier limiting the out diffusion of these substrate elements is being investigated in this study.

Silicon nitride (Si_3N_4) films deposited on SS foils are being investigated as the barrier layer, to reduce or inhibit the diffusion of substrate impurities into the solar cell. Thin film CdTe solar cells have been fabricated and characterized by AFM, XRD, SEM, ASTM D3359-08 tape test, current-voltage (I-V) and spectral measurements.

My individual contributions to this work include the Molybdenum (Mo) development, the adhesion studies, the silicon nitride (Si_3N_4) barrier studies, and EDS and SEM lines measurements and analysis of substrate out-diffused impurities. The rest of my colleagues focused on the development of CdTe, CdS, ZnTe, the $CdCl_2$ heat treatment, and other back contact interlayer materials.

Chapter 1

Introduction

1.1 Historical Overview of Photovoltaics

The conversion of sunlight directly into electricity using the photovoltaic properties of suitable materials is a distinctively green but underutilized energy conversion process. Solar cell technology has been historically used in providing electrical power for spacecraft, and more recently for terrestrial systems. The driving force for the recent and ongoing technological development is the realization that the traditional fossil energy resources, coal, oil and gas, are not only limited, but are harmful to the environment, depleting the ozone layer through the emission of carbon dioxide. The use of sunlight offers a favorable and promising alternative to the worldwide energy problems.

The photovoltaic effect of the solar cell operation was discovered in 1839 by a French physicist, and one out of a family of four generations of scientists, Alexandre-Edmond Becquerel. He was the father of Henri Becquerel, a French physicist, Nobel laureate, and one of the discoverers of radioactivity. The first solid state materials that showed a significant light-dependent voltage between two contacts were selenium in 1876 and later cuprous oxide [1]. Almost simultaneous with the beginning of silicon

solar cell technology was the first development of cuprous sulfide/cadmium sulfide heterojunctions, which served as the basis for intense research on thin-film solar cell devices [2]. The solar cell using a diffused silicon p-n junction was first developed by Chapin, Fuller, and Pearson in 1954 [3]. Subsequently, the cadmium-sulfide solar cell was developed by Raynolds et al [2]. The demand for a reliable, long-lasting power source was the major reason for the application of solar cells, and by 1958 the first silicon solar cells were used in spacecraft.

Interest arose in solar cells as an alternative energy source for terrestrial applications in the mid-1970s after the political crisis in the Middle East, the oil embargo, the realization that fossil fuel sources were limited, and recently the current political crisis in the Middle East, and the latest war with Iraq. We peaked in domestic oil production in the 1970's and as far as crude oil is concerned, we will never again produce as much domestic oil as we did at the turn of the century in 2000, even if we drill as hard as we can in the Artic National Wildlife Refuge and offshore combined. The gap between the United States oil consumption and production will only continue to widen. The cost target for electricity from a photovoltaic plant operating for 30 years was established in 1986 to be equal to about 0.06 US$/kWh. It was estimated that this requires module efficiencies in the range of 15% to 20% for a flat panel system and 25% to 30% for a system operating under concentrated sunlight [1].

Photovoltaics has experienced extraordinary growth during the last few years with overall growth rates between 30% and 40% making further increase of production facilities and attractive investment [4]. In 2008, the world-wide photovoltaic industry delivered some 6,941 MW of photovoltaic generators shown in Figure 1 [5].

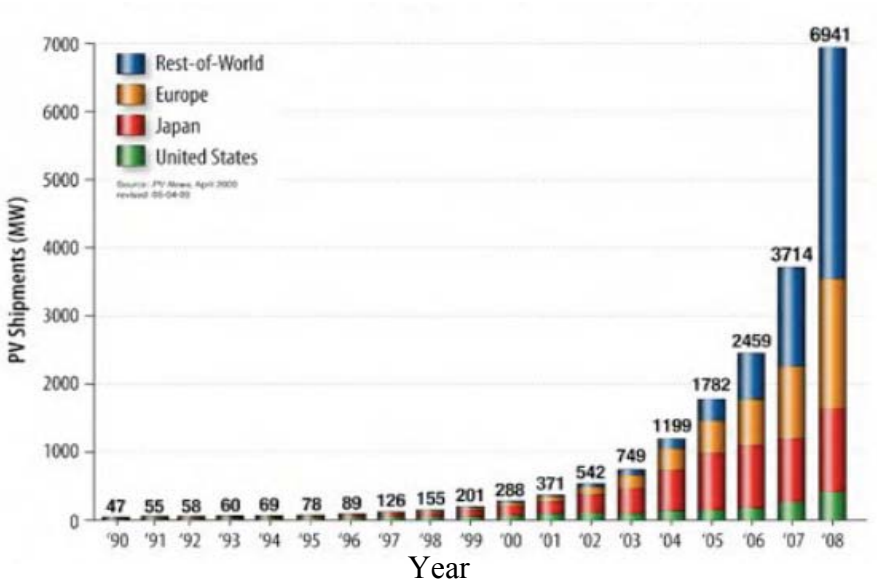


Figure 1. World PV production growth. [5]

1.2 Thin Film Solar Cells Current Status

The photovoltaics' (PV) market is dominated by crystalline silicon solar modules which require thicknesses of approximately 200-300 μm and high energy intensive processes. Expensive materials and processes limit the potential for future long term cost reductions. Thin film polycrystalline low cost alternatives to silicon have emerged. Thin film solar cells require only a few microns of film thickness and less energy intensive processes. The market share for thin-film PV in the US continues to grow rapidly and was reported at more than 44% in 2006, as illustrated in Figure 2 [6].

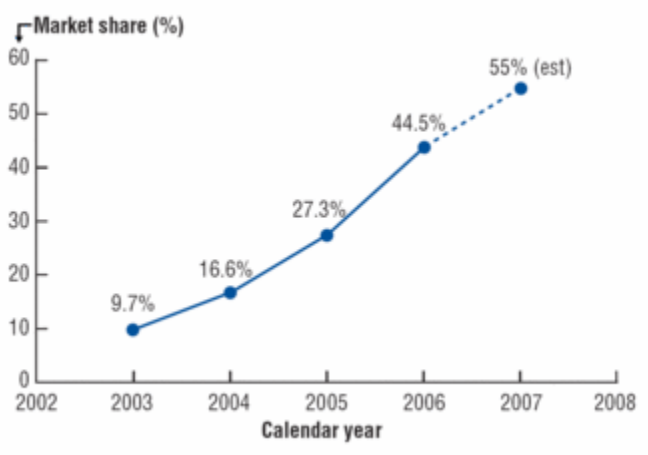


Figure 2. Market share for thin-film PV in the US. [6]

The typical range of the thin-film technology is a layer of about 1-μm thickness or less. A variety of thin-film deposition techniques are available, offering great flexibility for the thin-film preparation. Other advantages of thin film solar cells are that less material is required and that the thin layers can be deposited on many different substrates. Thin films can be deposited either as polycrystalline, nanocrystalline, or amorphous layers.

The choice of materials for photovoltaic conversion is based on a number of requirements including:

1. A direct band gap with nearly optimum values for either homojunction or heterojunction devices.
2. A high optical absorption coefficient, which minimizes the requirement for high minority carrier lengths.

3. The possibility of producing *n*- and *p*-type material, so that the formation of homojunction as well as heterojunction devices is feasible. Generally *p*-type material is preferred because electrons in many cases have a higher mobility, and the materials therefore exhibit a higher minority carrier length. Another reason is that most suitable window materials have an n- type character, and a *p*- type absorber is needed in a heterojunction device.
4. A good lattice and electron affinity match with large band gap (window) materials such as CdS or ZnO so that heterojunctions with low interface state densities can be formed and device limiting conduction band spikes can be avoided.

These requirements are fulfilled by a number of II-VI compounds. For photovoltaic applications, only cadmium and zinc compounds are directly suitable. They are direct band gap semiconductors, with high absorption coefficients and can be used as thin-film materials. Cadmium telluride (CdTe) is a leading thin film photovoltaic material due to its near ideal band gap of 1.45 eV, its high optical absorption coefficient and availability of different device fabrication methods, for solar energy conversion. A thin film of CdTe with thickness of approximately 2 μm will absorb nearly 100% of the incident radiation [7].

The status the thin film CdTe/cadmium sulfide (CdS) solar cell is 16.5% efficiency for devices on conducting glass substrates [8], as illustrated in Figure 3, 7.8% efficiency for devices on flexible metallic substrates [9] and 8.6% efficiency for devices on flexible polymer substrates [10].

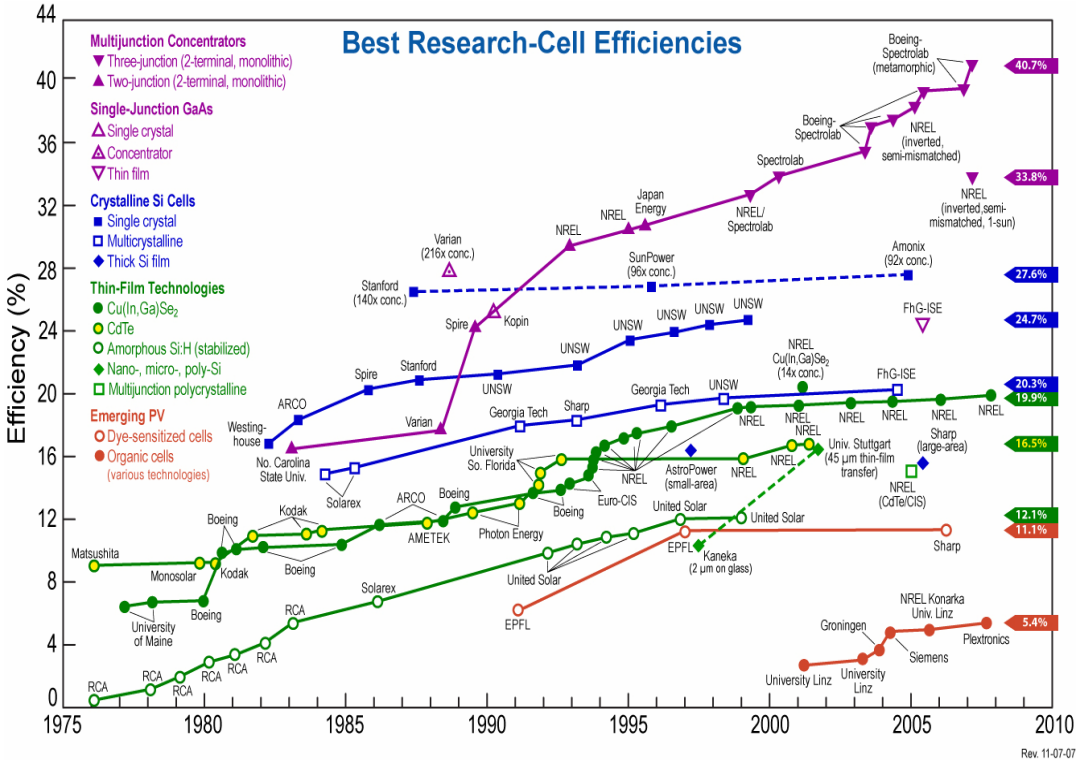


Figure 3. Best research solar cell efficiencies. [8]

1.3 Solar Cells on Flexible Substrates: Recent Progress

Conventional polycrystalline thin film solar cells are usually manufactured on thick glass substrates and offer no weight advantage or shape adaptability for curved surfaces. Producing thin film solar cells on flexible metal foil substrates offers several advantages for space as well as terrestrial applications. CdTe solar cells on glass substrates have efficiencies exceeding 16%, and recent development CdTe solar cells on flexible metal foils in a substrate configuration report efficiencies in the range of 3.8 to 8% [9, 11, 12]. Challenges in the development of CdTe devices on metallic substrates is the formation of an effective ohmic contact with CdTe and the incorporation of an

additional buffer layer as an ohmic contact to increase the cell efficiency. The criteria of matching thermal expansion coefficients and work function, limit the choice of substrate and contact materials. An additional consideration is the change to the ohmic contact properties, as a result of diffusion of impurities during the $CdCl_2$ annealing treatment and from the stainless steel substrate. Recent progress on the fabrication technology of CdTe/CdS solar cells on flexible metallic substrates is reviewed, from three different groups:

1. The University of Toledo with 7.8% efficiency solar cells
    a. Mo substrate sheet 100 μm thick
    b. CdTe, CdS, ZnTe:N, ITO RF sputtered
    c. Mo - 250°C @ 18mTorr Ar
    d. CdTe & CdS – 36 – 38 W RF Power
    e. Vapor $CdCl_2$, 30 min. 390°C anneal
    f. 1,000 Å ITO

2. The University of Kentucky and the University of Texas with 6% efficiency solar cells
    a. Mo foil - 0.1 mm thick
    b. Cu & Te evaporation - 500Å
    c. CdTe thermal evaporation, T_{sub} = 220°C, 5 μm
    d. $CdCl_2$ solution and anneal @ 300 - 500°C for 1 – 4 hours
    e. CdS – thermal evaporation (2 CdS layers)

f. $CdCl_2$ treatment, anneal and In doping

g. ITO, ZnO RF sputtered (temperature dependencies)

h. In – thermal evaporation or solder

3. National Autonomous University of Mexico with 3.5% efficiency solar cells

a. Mo foil

b. CSS CdTe - T_{source} = 670°C, T_{sub} = 570°C

c. Saturated solution of $CdCl_2$, anneal at 400°C

d. Br-methanol rinse

e. CBD CdS at 90°C

f. ITO RF sputter

g. In – solder

1.3.1 University of Toledo: 7.8% Efficiency

This group has achieved AM1.5 conversion efficiencies of 7.8% on 0.05 cm^2 area devices [9]. Their best cells had a nitrogen-doped ZnTe layer between the Mo and the CdTe. Mo/ZnTe/CdTe/CdS/ITO cells were fabricated on Mo sheet substrates 100 μm thick. The device structure is shown in Figure 4. The polycrystalline CdTe, CdS, ITO, and ZnTe films were grown using planar magnetron radio-frequency (RF) sputtering. The Mo temperature during growth was 250°C; 18 mTorr of argon sputter gas flowing at a rate of 27 sccm and 36 to 38 W of RF power were used for both CdS and CdTe growth. The cells received a standard 30 min. annealing at 390°C in a vapor $CdCl_2$ atmosphere

and then a 100 nm thick ITO top electrode sputtered through a mask to define typically 16 cells on the substrate. The use of a 150 nm ZnTe:N layer resulted in some improvement in the device performance.

The spectral quantum efficiency (QE) of a Mo substrate cell is compared with a glass substrate cell in Figure 5. The QE of the substrate cell shows little evidence of consumption of CdS, and a much sharper turn-on near 530 nm, consistent with little alloying. A small amount of sulfur (S) alloyed into CdTe lowers the band gap [13]. The Mo substrate cell shows a response cut-off at about 10 nm less than for the glass superstrate cell. Figure 6 shows a current-voltage curve of a substrate cell. The very severe roll-over in the first quadrant, indicate the presence of a reverse diode or blocking diode.

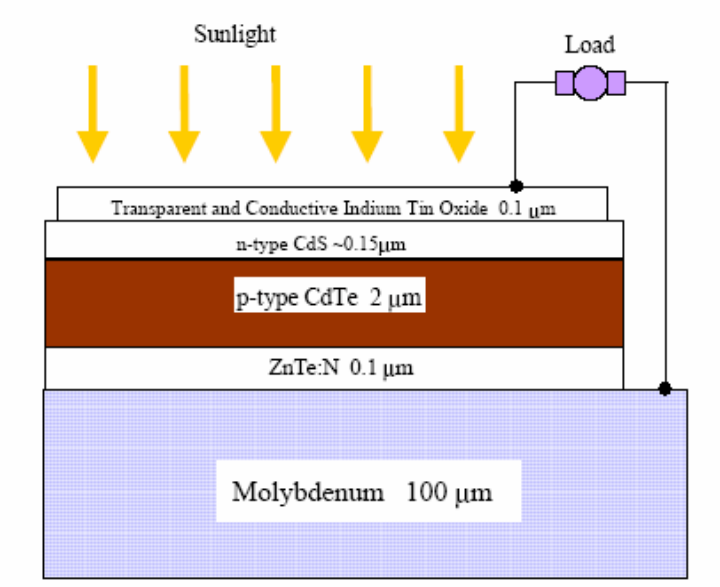


Figure 4. Device structure of the substrate solar cell. [9]

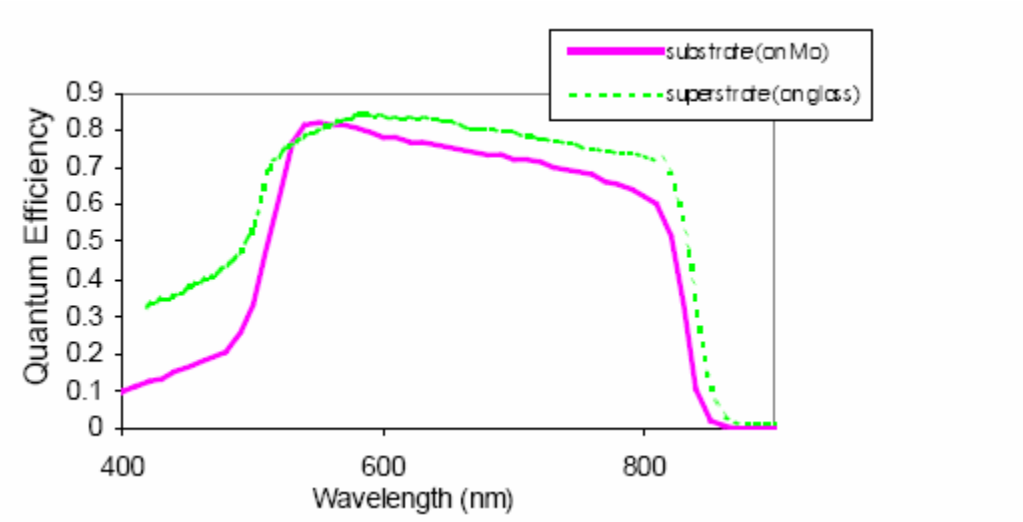


Figure 5. Comparison of the quantum efficiency curves of the substrate and superstrate cells. [9]

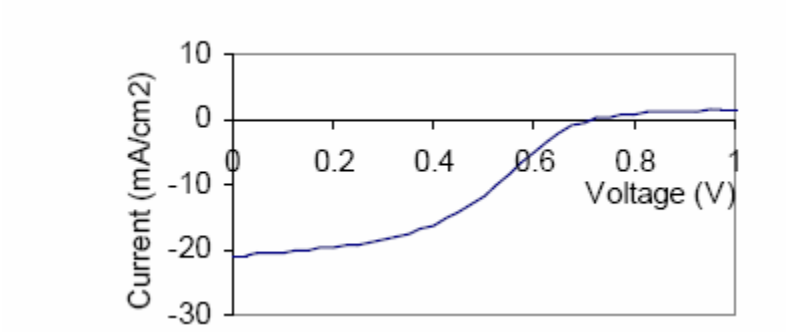


Figure 6. The I-V curve of a typical substrate cell. [9]

1.3.2 University of Kentucky & University of Texas: 6% Efficiency

The starting substrate consisted of a molybdenum foil of thickness 0.1 mm. CdTe was deposited by thermal evaporation; the substrate temperature during deposition was 220°C. Typical thickness of CdTe is 5 μm. After deposition, CdTe is treated with a $CdCl_2$

solution and annealed at temperatures between 300°C and 500°C for 1–4 h. In order to ensure an ohmic contact between Mo and CdTe, interlayers (approximately 50nm thick) of Cu and Te are evaporated onto the Mo substrate prior to CdTe deposition.

Next, CdS films are deposited by thermal evaporation and are subjected to $CdCl_2$ treatment, annealing and indium doping. The top contacting material is made by sputtering ZnO, ITO or a combination of ZnO and ITO followed by the thermal evaporation or soldering of an indium (In) grid. A schematic of the CdTe–CdS solar cell is shown in Figure 7. It has been observed that at anneal temperatures of 550°C for 2 h, CdTe does not peel away from Mo foil nor does it form blisters or bubbles [14].

Thin Cu and Te layers are put down before CdTe is deposited on metal. Tellurium can dope CdTe and make it heavily p-type, which facilitates tunneling. Similar effects can also be obtained with copper. Also, Cu and Te can form $Cu_{2-x}Te$ between Mo and CdTe and make tunneling more effective. The CdTe evaporation is performed at a relatively low temperature (~220°C), post deposition annealing is essential for achieving good quality CdTe. The annealing temperature, time, atmosphere and pre-annealing $CdCl_2$ treatment have significant effects on the material and electrical properties of CdTe.

The ITO and ZnO:Al were sputtered on the metal substrate CdS–CdTe solar cell. The sputter power for ITO was 40W and for ZnO:Al, the power was 80 W. Three TCO configurations were evaluated. These were:

1. 500–600 nm ITO layer;
2. 500–600 nm ZnO:Al layer; and
3. 50–70 nm ZnO:Al + 500–600 nm ITO layer.

The experimental results are shown in Table 1. From Table 1, it can be seen that when sputtering was done at room temperature, the V_{oc} of solar cell remained at its original level or improved. When the substrate temperature during TCO deposition was higher than 150°C, the V_{oc} decreased by about 300 mV. When ITO was sputtered onto CdS at 350°C, the cell's V_{oc} was reduced to almost zero. These results indicate that the deposition of TCO layers should be done at low temperature in order to maintain the original Voc of the solar cell.

Higher open-circuit voltages are achieved when two CdS layers (separated by an air anneal) are used instead of a single CdS layer. This indicates the importance of cross diffusion of the Te and S across the CdS–CdTe interface. The high series resistance of this solar cell, attributed to the top transparent contact, continues to be the limiting factor in cell performance. Due to this high series resistance, the fill factor is low and the cell efficiency has been limited to 6% in spite of the relatively high open circuit voltage of 824mV achieved in these cells.

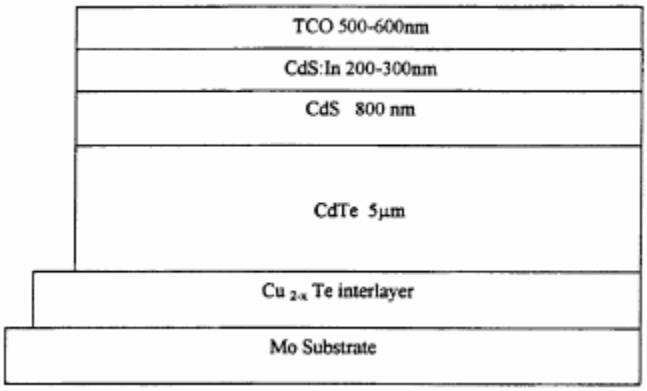


Figure 7. The solar cell CdS – CdTe structure. [14]

Table 1. Effects of sputter depositing TCO on the open-circuit voltage of the cell. [14]

Sample#	V_{oc} before sputter (mV)	TCO structure	Substrate temperature (°C)	V_{oc} after sputter (mV)	R_{se} (mV) (Ωcm^2)
MB65-3	520	ITO	Room temperature	550	460
MB65-3	520	ITO	150	230	240
MB65-12	570	ITO	200	240	230
MB63-9	640	ITO	250	290	140
MB66-1	680	ITO	300	320	55
MB65-2	540	ITO	350	24	0.26
MB65-12	570	ZnO:Al	Room temperature	620–630	>999
MB64-15	418–430	ZnO:Al	250	290–300	540
MB64-6	472–479	ZnO:Al	300	320	170
MB63-9	483	ZnO:Al+ITO	ZnO: Room temperature ITO: 150	370	130
MB63-14	498	ZnO:Al+ITO	ZnO: Room temperature ITO: 250	260	34
MB63-10	510	ZnO:Al+ITO	ZnO: Room temperature ITO: 350	250	

1.3.3 National Autonomous University of Mexico: 3.5% Efficiency

The CdTe thin films were developed on flexible Mo substrates by CSS. The source of CdTe was a thick film of stoichiometric CdTe evaporated on a quartz glass. The films were prepared at a substrate temperature of 570°C and a source temperature of 670°C. The films were treated with a saturated solution of $CdCl_2$ and annealed at 400°C in dry air. After the annealing, the CdTe films were rinsed with 0.2 vol.% Br–methanol solution for 2 seconds to clean the CdTe surface, followed by a thorough rinsing in de-ionized water in an ultrasonic bath.

CdTe/CdS junctions were prepared by depositing approximately 0.1 μm thick CdS layer onto the CdTe substrates from a chemical bath containing 0.033M cadmium acetate, 1 M-ammonium acetate, 28–30% ammonium hydroxide and 0.067M thiourea.

The bath was maintained at a constant temperature of 90°C and continuously stirred during the deposition. The CdTe/CdS device was washed with de-ionized water and dried in air and later annealed at different temperatures in air. The top contacting material is made by sputter depositing ITO on the annealed CdTe/CdS surface followed by soldering of an indium (In) grid.

The XRD spectrum of the as-deposited CdTe film is shown in Figure 8. It can be seen that the film is crystalline, but does not have any preferred orientation for the crystallites. The SEM image, Figure 9, shows that the film surface contains voids and the grain size is in range 1–2 μm. The AUGER depth profile analysis revealed that the composition is uniform throughout the thickness of the film and the percentage composition of the film is 50.5% Te and 49.5% Cd.

The I–V characteristics under illumination of a typical device annealed at 400°C is shown in Figure 10. The device parameters were estimated as $V_{oc} = 0.5$ V, $J_{sc} = 10.6$ mA/cm^2, FF = 0.40 and $\eta = 3.5\%$. Figure 11 and Figure 12 demonstrate the variation of the V_{oc} and the J_{sc} of the devices with the annealing temperature. At each temperature the devices were annealed for 30 min. The maximum value of the V_{oc} and J_{sc} was obtained for devices annealed at 400°C indicating that the optimum temperature for the annealing process of the CdTe/CdS junction is near to 400°C.

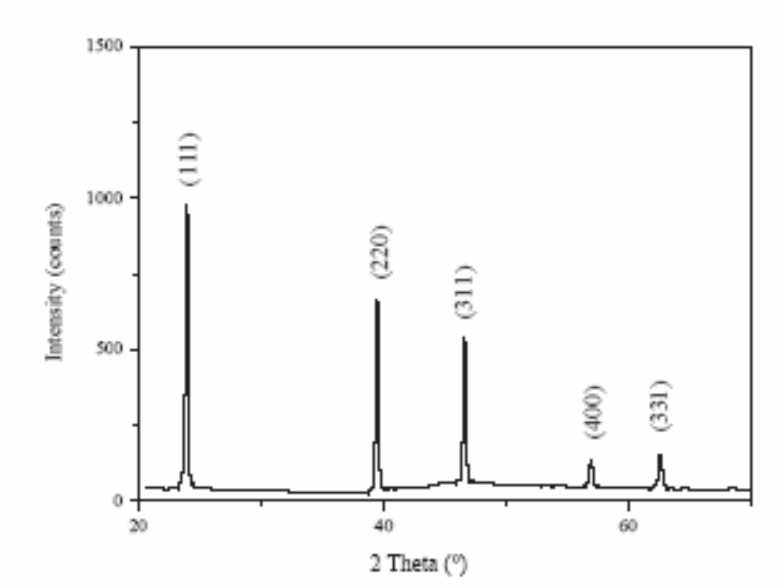


Figure 8. XRD spectrum of the as-deposited CdTe film on Mo substrate. [12]

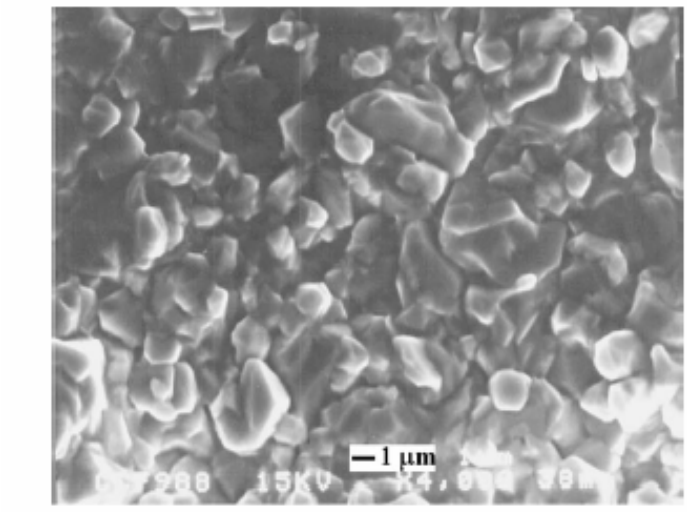


Figure 9. SEM image of the as-deposited CdTe thin film. [12]

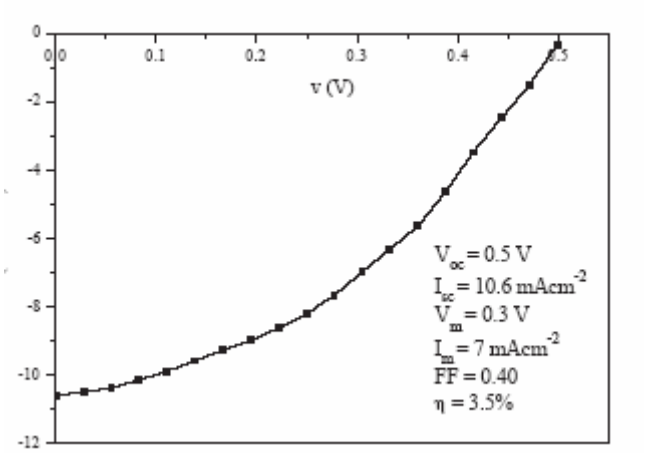


Figure 10. I-V characteristic of a CdTe/CdS solar cell developed on flexible Mo substrate. [12]

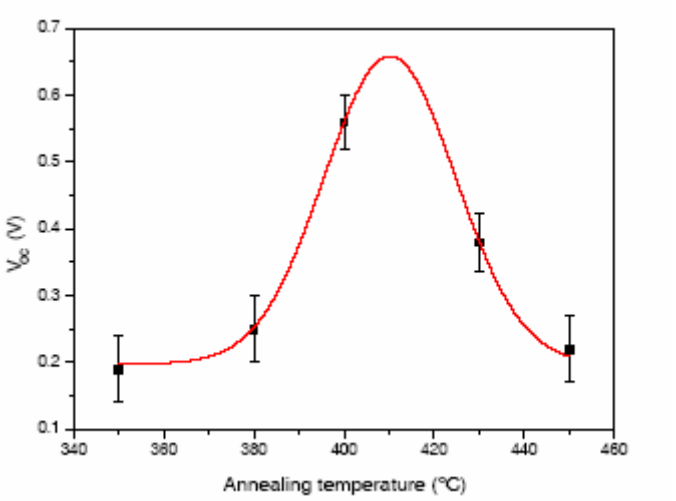


Figure 11. Graph showing the dependence on V_{oc} on the annealing temperature on the CdTe/CdS device. The markers are experimental data and the line is a guide to the eye. [12]

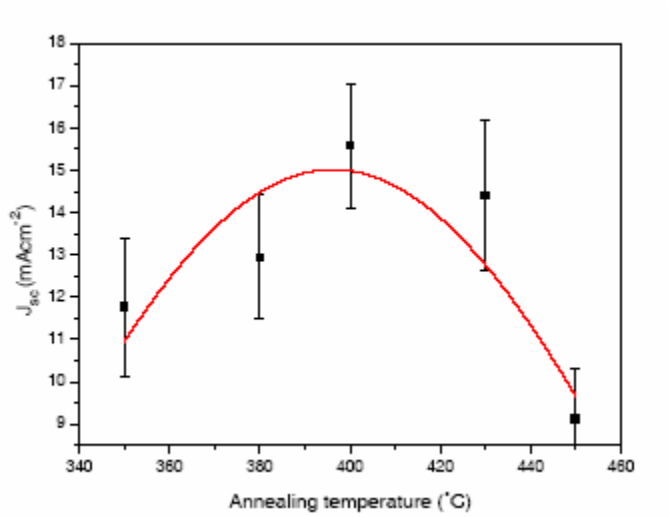


Figure 12. Graph showing the dependence of J_{sc} on the annealing temperature of the CdTe/CdS device. The markers are experimental data and the line is a guide to the eye. [12]

1.4 Objectives and Motivation

Research into photovoltaic alternatives is imperative to make the technology competitive. This includes the development of low-cost techniques, higher efficiency cells using new materials and cell concepts, and thin films that require less material. Essential to any option is successful tailoring of the semiconductor material and the control of the electro-optical properties during each processing step. For thin-film CdTe technology, five critical research and development issues need to be addressed:

1. higher cell efficiencies, ≈ 20%
2. thinner CdTe cells

3. standardization of equipment for deposition of CdTe
4. higher module efficiency
5. back-contact stability
6. control of uniformity over a large area.

The conventional polycrystalline thin film solar cells are usually developed on thick glass substrates and offer no weight advantage or shape adaptability for curved surfaces. The primary objective of this research is to transform the standard process/product design of CdTe solar cells and modules from a glass-to-glass superstrate configuration, into a metallic foil substrate configuration using a high throughput process, close-spaced sublimation, illustrated in Figure 13. This approach has significant manufacturing and product option advantages:

1. the potential to fabricate cells on flexible and lightweight substrates will result in an entire new line of products,
2. the use of high temperatures for the fabrication of solar cells leads to the formation of more efficient junctions, and
3. NASA's light weight space applications and satellite systems.

A major challenge associated with the flexible substrate CdTe solar cell, Figure 14, will be achieving strong adhesion of the solar cell structure onto the metallic foil. This research studies of adhesion of suitable metallic films onto a foil substrate, and the development and optimization of the deposition process and substrate preparation conditions that result in strong film adhesion on the foil substrate.

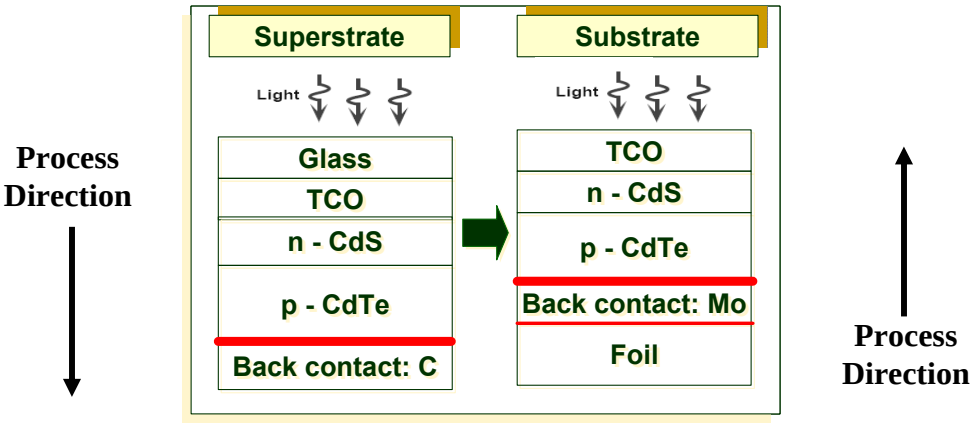


Figure 13. Glass superstrate to flexible substrate process transformation.

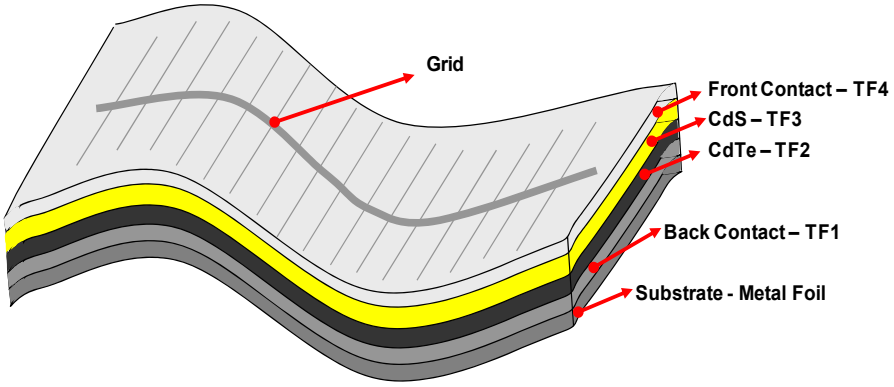


Figure 14. Flexible substrate CdTe solar cell.

For producing highly efficient thin film CdTe/CdS solar cells, the back contact, molybdenum has to be relatively free of residual stresses. Residual stress can result in undesirable effects which impact the overall solar cell performance, including, excessive deformation, fracture, delamination and microstructural changes in the materials. If films

lift from the substrate, device failure can result, and thereby making poor adhesion a reliability problem. Therefore, both excellent adhesion and minimum stress are required of a CdTe/CdS thin film solar cell device.

An important issue associated with the fabrication of CdTe solar cells is the formation of a low resistance back contact. To form an ohmic contact on p-CdTe, metals with a work function greater than 5.7 eV are required. There are no low cost metals available and the result is the formation of a Schottky barrier at the back contact. An alternative approach is the development of a pseudo-ohmic contact to achieve tunneling. Buffers can be deposited between CdTe and Mo to achieve a pseudo-ohmic contact. This work also focuses on the investigation of buffers such as ZnTe and Sb_2Te_3 in the development of efficient back contacts for CdTe thin film solar cells deposited on flexible foil substrates. Solar cells were fabricated using ZnTe and Sb_2Te_3 as buffer layers. Buffer film thicknesses and deposition process conditions were optimized, with all other conditions of other layers remaining constant, and device characteristics studied.

Thin stainless steel (SS) foils are used as the substrate for the development of CdTe solar cells because of the SS foil's material properties, high temperature stability, commercial availability and cost. A potential problem with the use of SS foils as the substrate is the diffusion of iron (Fe), chromium (Cr) and other elemental impurities into the layers of the solar cell device structure during high temperature processing. A diffusion barrier limiting the out diffusion of these substrate elements is being investigated in this study. Silicon nitride (Si_3N_4) films deposited on SS foils are being investigated as the barrier layer, to reduce or inhibit the diffusion of substrate impurities into the solar cell. Si_3N_4 coefficient of thermal expansion (CTE) of $3.1x10^{-6}$/°K is close

to both the back contact layer Molybdenum, with a CTE of $5.1x10^{-6}$/°K and the absorber CdTe, with a CTE of $5.9x10^{-6}$/°K, minimizing thermal expansion mismatch in the device.

It has already been shown by others developing CIGS cells on stainless steel substrates, that substrate impurities like Fe and Cr in the cell's absorber can lead to reduced cell efficiencies [15]. In this study, the effect of the Si_3N_4 barrier layer is being evaluated for its effect on cell efficiency and overall device performance. The optimum Si_3N_4 barrier layer thickness is also being determined. Thin film CdTe cells were fabricated with and without a Si_3N_4 barrier layer. Preliminary results show an improvement in the V_{OC} of cells fabricated with a 0.1 μm thick Si_3N_4 barrier layer. The thin film CdTe solar cells have been characterized by XRD, SEM, Secondary Ion Mass Spectrometry (SIMS) depth profiles, current-voltage (I-V) characteristics and spectral response.

Chapter 2

Principles of Solar Cells

2.1 Solar Spectrum

The radiative energy output from the sun derives from a nuclear fusion reaction. This energy is emitted primarily as electromagnetic radiation in the ultraviolet to infrared and radio spectral regions (0.2 to 3μm). The spectral distribution of the radiation emitted from the sun is determined by the temperature of the surface (photosphere) of the sun, which is about 6000°K. The wavelength distribution of the sunlight (power per unit area and per unit wavelength) follows approximately the radiation distribution of a black body at this temperature, as shown in Figure 15 [16, 17]. The deviations at certain wavelengths are due to absorption effects in the sun's atmosphere.

The total energy per unit area integrated over the entire spectrum and measured outside the earth's atmosphere perpendicular to the direction of the sun is essentially constant. This radiation power is referred to as the solar constant or air mass zero (AM0) radiation. Measurements taken at high altitudes have yielded the currently accepted average value of 1.353 kW/m^2 [18]. The spectral distribution is changed considerably when the sunlight penetrates through the earth's atmosphere. When the sky is clear, the light intensity is attenuated by at least 30% because of scattering at molecules, aerosols, and dust particles, and absorption by the atmosphere's constituent gases, such as water

vapor, ozone, or carbon monoxide. The attenuation mechanisms are wavelength-dependent, which explains the strong absorption bands in the spectral distribution measured at the earth's surface. The scattering of light increases with decreasing wavelength so that shorter wavelengths in the original sun beam experience more scattering than longer wavelengths.

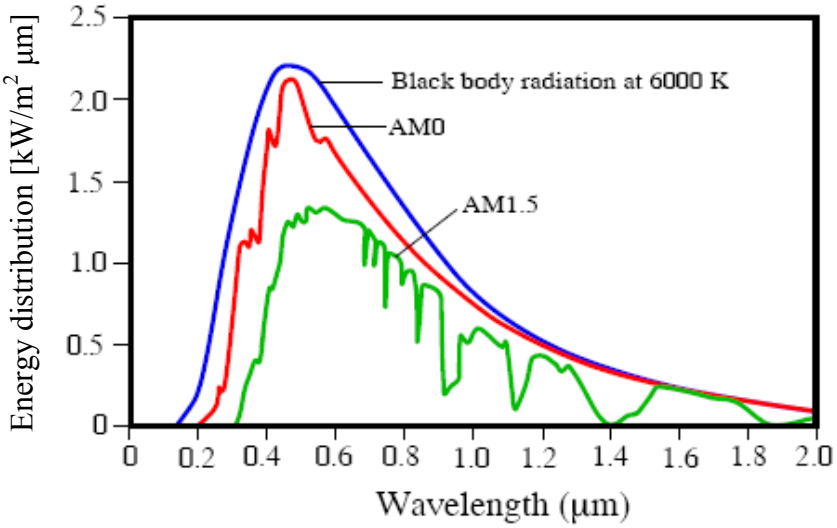


Figure 15. Spectral distribution of sunlight. Shown are the radiation outside the earth's atmosphere (AM0) and at the surface (AM1.5). [17, 19]

The secant of the angle between the sun and the zenith (sec θ) is called the air mass and measures the atmospheric path length relative to the minimum path length when the sun is directly overhead. Outside the earth's atmosphere, the air mass zero condition (AM0) is constant. The AM0 spectrum is the relevant one for satellite and space vehicle applications. The AM1 spectrum represents the sunlight at the earth's surface when the sun is at zenith; the incident power is about 925 W/m^2. The AM2

spectrum is for θ = 60° and has an incident power of about 691 W/m^2. Air mass 1.5 conditions (sun at 45° above the horizon) represent a satisfactory energy-weighted average for terrestrial applications. The total incident power for AM1.5 is 844 W/m^2. In the U.S. photovoltaic program, the spectral distribution for AM1.5 radiation has been adopted as a terrestrial standard to allow meaningful comparison of different solar cells tested at different locations. Normalized AM1.5 of 1 KW/m^2 is used in our lab testing of solar cells.

2.2 Heterojunction Devices

A heterojunction is a junction formed between two dissimilar semiconductors. There should be an improvement of the efficiency of solar cell device if it consists of materials with different band gap energies which match different parts of the solar spectrum. This concept is realized in a heterojunction device formed between semiconductors with different band gap energies. Figure 16 [20, 21] shows the energy-band diagram of two isolated pieces of semiconductors. The two semiconductors have different bandgaps E_g, different permittivities ϵ, different work functions ϕ_m, and different electron affinities χ. Work function and electron affinity are defined as that energy required to remove an electron from the Fermi level E_F and from the bottom of the conduction band E_C, respectively, to a position just outside the material (vacuum level). The difference in energy in the conduction-band edges in the two semiconductors is represented by $\Delta E_C = (\chi_1 - \chi_2)$ and that in the valence-band edges by ΔE_V.

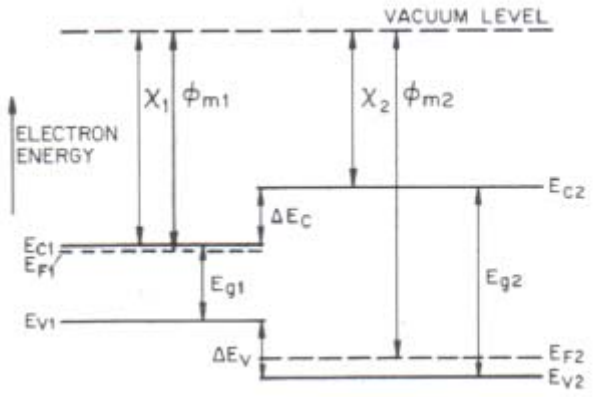


Figure 16. Energy-band diagram for two isolated semiconductors in which space-charge neutrality is assumed to exist in each region. [20, 21]

When a junction is formed between these semiconductors, the energy-band profile at equilibrium is a shown in Figure 17 [22] for an *n*-on-*p* heterojunction. Since the Fermi level must coincide on both sides in equilibrium and the vacuum level is everywhere parallel to the band edges and is continuous, the discontinuity in conduction band edges (ΔE_C) and valence-band edges (ΔE_V) is invariant with doping in those cases where E_g and χ are not functions of doping. The total built-in potential V_{bi} is equal to the sum of the partial built-in voltage ($V_{b1} + V_{b2}$), where V_{b1} and V_{b2} are the electrostatic potential supported at equilibrium by semiconductors 1 and 2, respectively.

An *n*-on-*p* CdS/CdTe band diagram is shown in Figure 18 [23]. In Figure 18, the solid line represents the model of zero band offset between *n*-type CdS and *p*-type CdTe, while the dashed and dotted lines illustrate the models of cliff and spike offsets respectively. The open arrow shows the electron-hole pair generation. The solid arrows illustrate the electron and hole transport in including barrier penetration by activation and

tunneling. The material with the larger band gap E_{g1}, *n*-type CdS, is on the top. Light with energy less than the band gap energy E_{g1} but greater than E_{g2} passes through the first semiconductor, which acts as a window, and will be absorbed by the second semiconductor, *p*-type CdTe. Carriers generated in the depletion region and within a diffusion length of the junction are collected. Light with photon energies larger than E_{g1} will be more efficiently utilized by the first semiconductor. The advantages of heterojunction solar cells over conventional cells include enhanced short wavelength response, lower series resistance, if the first semiconductor can be heavily doped, and higher irradiation resistance.

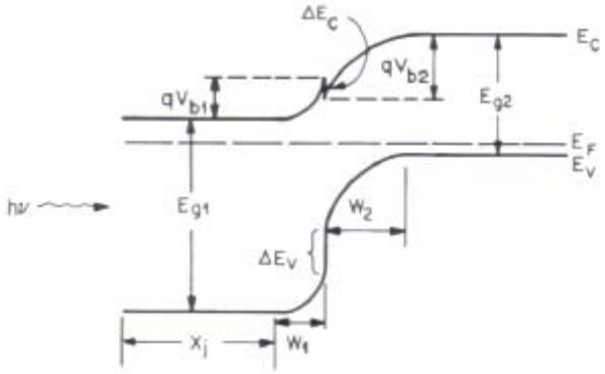


Figure 17. Energy-band diagram of an *n*-on-*p* heterojunction in thermal equilibrium. [22]

A negative ΔE_C produces a spike in the conduction band which is undesirable for photovoltaic applications. The spike impedes the flow of minority carriers across the junction from the *p*-type to the *n*-type regions, and the photocurrent will be reduced. Such spikes can, however, be avoided by a suitable combination of electron affinities and band gap energies [24]. For heterojunctions, there is the inherent problem that the crystal structure changes across the junction and an interface is formed between the two

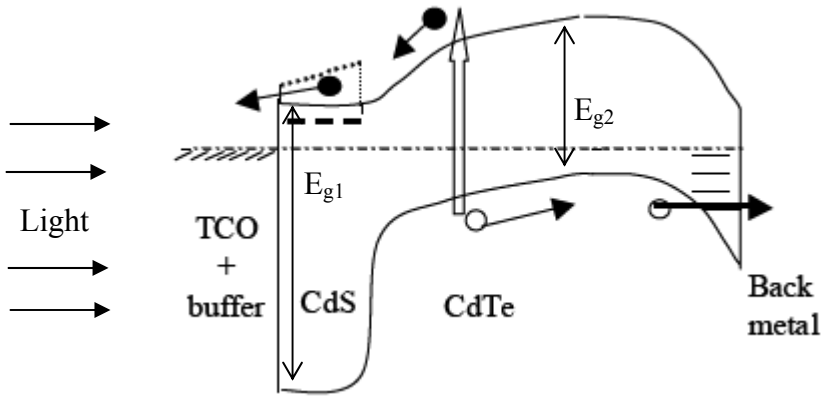


Figure 18. Schematic band structure of an n-CdS/p-CdTe solar cell. [23]

semiconductors. Interfaces can be efficient recombination centers because they introduce deep trap levels in the band gap. They can also provide sites for quantum mechanical tunneling processes, which is important for current loss mechanisms across the junction. In both cases, the interface traps degrade the performance of the solar cell, and it becomes essential to produce heterojunctions with a low density of interface traps. The density of interface traps is possibly related to the degree of mismatch between the crystal lattices of the two semiconductors. Therefore, the requirements for a good *n*-on-*p* heterojunction solar cell are a small ΔE_C and a good lattice match.

2.3 Absorption of Light in Solar Cells

The light-generated current I_L is determined by the absorption behavior of the semiconductor. The fraction of incident light $D = 1 - R$ that actually penetrates the

absorbing material can be calculated from the complex refraction index $n_c = n - i\kappa$, where κ is the extinction coefficient and the reflectivity R given by

$$R = \frac{(n-1)^2 + \kappa^2}{(n+1)^2 + \kappa^2} \tag{1}$$

where $n(\lambda)$ and $\kappa(\lambda)$ are functions of the wavelength λ of the incident light. For many semiconductors, a considerable fraction of light is reflected. Decreasing R improves the efficiency of a solar cell. This can be achieved by an antireflection coating or by a textured structure of the surface.

The important process for photovoltaic conversion is the excitation of electrons from the valence into empty states of the conduction band, which can occur if the energy of the incident photons is larger that the band gap energy. The light passing through the material is absorbed then, and the number of generated electron-hole pairs depends on the number of incident photons $S_o(v)$ (per unit area, unit time, and unit energy) that can be calculated from the spectral distribution of the sunlight in Figure 15. The frequency v or the photon energy hv is related to the wavelength λ by the relation $\lambda\ [\mu m] = c/v = 1.24/hv\ [eV]$ where c is the speed of light. Inside the crystal the photon flux $S(x,v)$ decreases exponentially according to

$$S(x,v) = S_O(v)\exp(-\alpha x) \text{ with } \alpha(v) = \frac{4\pi\kappa\upsilon}{c} \tag{2}$$

where κ is the extinction coefficient and κ(λ) is a function of the wavelength λ of the incident light. The absorption coefficient $\alpha(v)$ is determined by the absorption process in the semiconductor and can be used to calculate the generation rate $G(x, v)$ of electron-

hole pairs (per unit time, volume, and energy) at a distance x from the semiconductor surface. The fraction of photons that penetrate into the crystal is given by $S_o(\nu)\ (1 - R)$; therefore, the number of electron-hole pairs generated per unit time in the volume between x and $x + \Delta x$ can be calculated from the derivative of (2) with respect to x:

$$G(x,\nu) = \beta(\nu)\alpha(\nu)S_O(\nu)(1-R)\exp(-\alpha(\nu)x) \tag{3}$$

The quantum efficiency $\beta(\nu)$ (of the internal photoeffect) takes into account that only a fraction of the absorbed photon energy generates electron-hole pairs. For many compound semiconductors it is observed that $\beta(\nu) \ll 1$ near the absorption edge. This is due to the formation of excitons or bound electron-hole pairs, which carry no charge and do not contribute to the conductivity. Near the absorption edge, where the values of $(h\nu - E_g)$ become comparable with the binding energy of an exciton, the Coulomb interaction between the free hole and electron must be taken into account. For $h\nu \lesssim E_g$ the absorption merges continuously into the absorption caused by the higher excited states of the exciton. When $h\nu \gg E_g$, higher energy bands participate in the transition processes, and complicated band structures are reflected in the absorption coefficient.

For photons with energies higher than the band gap energy, the electrons and holes carry excess (kinetic) energy that will be dissipated to the lattice until they occupy states near the band edges. The kinetic excess energy does not contribute to the photocurrent and is wasted in terms of energy conversion.

The absorption coefficient $\alpha(\nu)$ depends on the band structure of the semiconductor. In direct band gap semiconductors, the minimum of the conduction band and the maximum of the valence band occur for the wave vector in the Brillouin zone,

and the most likely transitions are between states close to the wave vector **k** = 0. A theoretical calculation of the probability for these direct (allowed) transitions gives the following result for the absorption coefficient α_d as a function of the frequency ν[25]:

$$\alpha_d(\nu) = \alpha_o \frac{\left(h\nu - E_g\right)^{1/2}}{h\nu} \tag{4}$$

E_g is the band gap energy, and α_o is a constant that is obtained from the calculation, but is usually fitted to experimental data.

Since both phonon absorption and emission are possible, the absorption coefficient is the sum of both processes. The absorption coefficients in both cases also depend on the temperature through the band gap energies, with usually decrease with increasing temperature.

High dopant impurity concentrations affect the shape of the band edges of a semiconductor. The distributions of valence and conduction band states can be considered "smoothed out" at the band edges (band tails), which effectively reduces the width of the band gap. A calculation of the band gap narrowing ΔE_g as a function of doping concentration N has been given by Lanyon and Tuft [26]:

$$\Delta E_g = \frac{3e^2}{16\pi\varepsilon}\left\{\frac{e^2 N}{\varepsilon KT}\right\}^{1/2} = \frac{3e^2}{16\pi\varepsilon L_D} \tag{5}$$

where ϵ is the permittivity of the semiconductor and L_D is the screening or Debye length. As is heavily doped semiconductors, the band structure of crystals with a high concentration of other lattice defects may also be characterized by band tails near the

band edges. The absorption behavior can also be changed by the high electrical fields which occur, for instance, in the space charge region of a *pn* junction. Figure 19 shows the absorption coefficient α plotted as a function of wavelength for CdTe and other semiconductor materials [27].

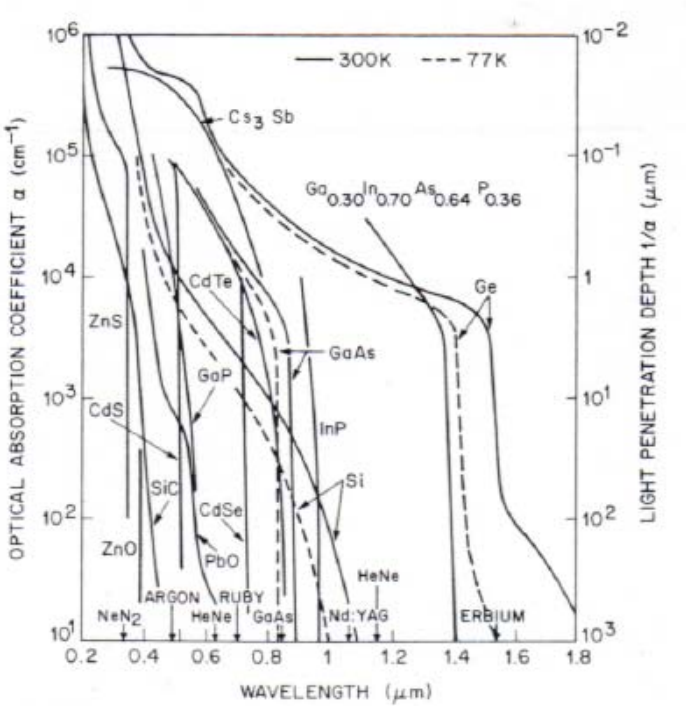


Figure 19. Optical absorption coefficients for CdTe and other semiconductors. [27]

2.4 Solar Cells under Illumination

A semiconductor under illumination shows an increased conductivity. For the photovoltaic conversion, it is necessary to separate the light-generated electrons and holes and collect them at external contacts. This requires an internal electric field, which can be

generated in semiconductors, by heterojunctions and homojunctions. The carrier concentrations for a non-degenerate semiconductor are given by

$$p = N_V \exp\left(\frac{E_V - e\phi - E_{Fp}}{KT}\right) \tag{6}$$

$$n = N_C \exp\left(\frac{E_C - e\phi - E_{Fn}}{KT}\right) \tag{7}$$

where the potential ϕ is related to the local electric field by E = -*grad* ϕ. N_C and N_V are the density of states of the conduction and valence band, respectively, E_{Fn} and E_{Fp} are the quasi-Fermi energies for electrons and holes, n are p are their concentrations, and e is the (positive) electron charge.

The basic equations that describe the flux of electrons and holes in a semiconductor under illumination are the current-density equations

$$\mathbf{J_p} = e\left(p\mu_p \mathbf{E} - D_p \nabla p\right) \tag{8}$$

$$\mathbf{J_n} = e\left(n\mu_n \mathbf{E} - D_n \nabla \mathrm{n}\right) \tag{9}$$

and the continuity equations

$$\frac{\partial p}{\partial t} = -\frac{1}{e}\nabla \cdot \mathbf{J_p} + G_p - \frac{\delta p}{\tau_p} \tag{10}$$

$$\frac{\partial n}{\partial t} = \frac{1}{e}\nabla \cdot \mathbf{J_n} + G_n - \frac{\delta n}{\tau_n} \tag{11}$$

The diffusion coefficients D_n and D_p are related to the mobility of the carriers μ_n, μ_p by the general Einstein relationship $D = (kT/e)\mu$. For light generated carriers, the generation rates for electrons and holes are equal to $G_n = G_p = G$.

Under normal illumination conditions for solar cells (AM 1.5), the product $G\tau$ is usually smaller than the majority carrier concentration; therefore, only the quasi-Fermi energy of the minority carriers is essentially changed. When an external electrical field **E** is applied and a current flows, the total current density **J** is given by

$$\mathbf{J} = \mathbf{J_p} + \mathbf{J_n} = \sigma\mathbf{E} \tag{12}$$

$$\sigma = e\left(p\mu_p + n\mu_n\right) \tag{13}$$

Solar cells require a *pn*-junction design illustrated in Figure 20 [1]. It consists of a shallow junction formed near the front surface, a front ohmic contact in the form of stripes and fingers, and a back ohmic contact that covers the entire back surface. The internal electric field $\boldsymbol{E} = -\nabla\cdot\boldsymbol{\phi}$ leads to an inhomogeneous distribution of electrons and holes, and the calculations of the currents requires the solution of the complete current-density equation and continuity equation. The potential $\boldsymbol{\phi(r)}$ is determined from Poisson's equation,

$$\Delta\phi = -\frac{e}{\varepsilon\varepsilon_o}\left(N_D(r) - N_A(r) - n + p\right) \tag{14}$$

where $N_D(\mathbf{r})$ and $N_A(\mathbf{r})$ are functions of the position and are usually equal to the concentrations of completely ionized acceptors and donors on each side of the junction. ϵ is the dielectric constant of the material, and ϵ_o is the permittivity of the vacuum.

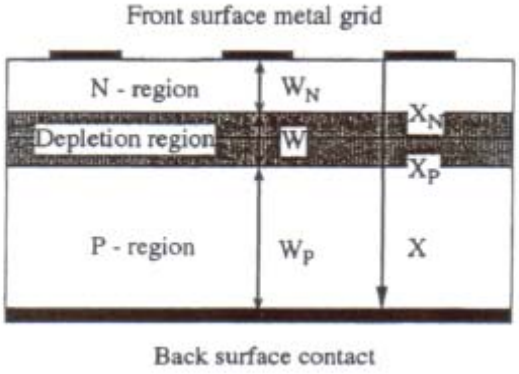


Figure 20. Schematic diagram of a *pn*-junction solar cell, defining basic parameters. [1]

For an abrupt *pn* junction with uniform doping concentrations on each side of the junction, the usual approximation is that within a certain width W the semiconductor is completely depleted from charge carriers. The depletion width W derived from (14) is

$$W = \sqrt{2\varepsilon\varepsilon_o V_B \frac{N_D + N_A}{N_D N_A}} \tag{15}$$

where the internal potential barrier $V_B = -e\phi_B$ is determined by the doping concentrations N_D and N_A on either side of the junction

$$V_B = KT \ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{16}$$

The potential ϕ_B (or diffusion voltage) determines the maximum voltage that can be obtained from an ideal *pn* junction solar cell.

When light is incident on the front surface and penetrates the crystal, the number of electrons and holes generated at a distance x from the surface is given by the

generation rate *G(x, v)*. In thermodynamic equilibrium, when no current flows, minority carriers reaching the edges of the depletion region are immediately accelerated by the electric field to the opposite side of the junction.

A current flows under illumination when the two sides of the *pn* junction are connected externally. The corresponding voltage drop *V* across the junction in forward bias direction is determined by the external load resistance. At the front and back surfaces, the excess concentrations are determined by the surface recombination

$$D_p \frac{\partial p}{\partial x} = S_p \delta p \quad \text{at } x = 0 \tag{17}$$

$$-D_n \frac{\partial n}{\partial x} = S_n \delta n \quad \text{at } x = W_p + x_p \tag{18}$$

W_p is the width of the *p*-base neutral region. This photocurrent would be collected from the front side of an *n-on-p* junction solar cell at a given wavelength, assuming this *n*-type region to be uniform in doping level, lifetime, and mobility. Some photocurrent generation also takes place in the depletion region. Since the electric field in this region is high, the generated electrons and holes are accelerated out of the region. If recombination is ignored, the photocurrent density in this case is equal to the number of photons absorbed. The total photocurrent I_L has to be calculated from the photocurrent density $J_L = J_p + J_n + J_{dp}$ by integrating over the entire solar spectrum, and is given by

$$I_L = A \int_{\upsilon_m}^{\infty} \left(J_p + J_n + J_{dp} \right) d\nu \tag{19}$$

where hv_m is the smallest photon energy corresponding to the absorption edge of the semiconductor, and A is the active area of the solar cell.

The photocurrent I_L is proportional to the light intensity that enters the crystal. The optical performance of a solar cell is frequently characterized by the normalized photocurrent $J_L(hv)$ as a function of the photon energy hv or wavelength λ. The external spectral response (or quantum efficiency) of the cell is the total photocurrent J_L divided by eS_o and the internal spectral response $SR(v)$ of the cell divided by $eS_o(1 - R)$, respectively:

$$SR(v) = \frac{J_p + J_n + J_{dp}}{eS_o(1-R)} \tag{20}$$

The maximum photocurrent that can be generated in a solar cell is given by I_L. A solar cell in an electrical circuit will produce a lower current which is determined by the external load resistance and the corresponding operation point on the current-voltage characteristics of the device. The total current I for an ideal pn-junction solar cell [22]:

$$I = I_S\left\{\exp\frac{eV}{KT} - 1\right\} - I_L \tag{21}$$

where the saturation current is given by (A is the active solar cell area)

$$I_S = eAN_C N_V\left\{\frac{D_n F_p}{L_n N_A} + \frac{D_p F_n}{L_p N_D}\right\}\exp\left(-\frac{E_g}{KT}\right) \tag{22}$$

The factors F_n and F_p account for the finite recombination velocity of electrons and holes at the front and back surfaces S_n and S_p.

2.5 Solar Cell Model

The solar cell can be represented by a current generator in parallel with a forward biased diode as illustrated in Figure 21 [28]. The current generated is proportional to the intensity of illumination, and the available power is drawn from terminals which are basically in parallel with the diode. The solar cell conversion efficiency relates to: (1) reflection – some of the incident light will be reflected from the surface of the cell; (2) wavelength – some of the light reaching the cell will have wavelength outside the spectral response of the cell and will not produce electron-hole pairs; (3) recombination – of the electron-hole pairs created, some will recombine before diffusing to the junction [29].

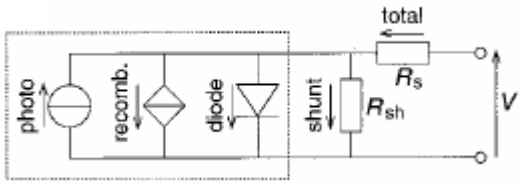


Figure 21. Equivalent circuit of a PV solar cell. [28]

The energy conversion process involves photogeneration and charge separation. A photovoltaic solar cell is basically a semiconductor diode. The semiconductor material absorbs the incoming photons and converts them to electron-hole pairs. In this photogeneration step, the decisive parameter is the bandgap energy E_{gap} of the semiconductor. In an ideal case, no photons with an energy $h\nu < E_{gap}$ will contribute to photogeneration, whereas all photons with an energy $h\nu > E_{gap}$ will each contribute the energy E_{gap} to the photogenerated electron-hole pair, with the excess energy ($h\nu$ - E_{gap}) being very rapidly lost because of thermalization.

In the second step of the energy conversion process, charge separation, the photogenerated electron-hole pairs are separated, with electrons drifting to one of the electrodes and holes drifting to the other electrode, because of the internal electric field created by the diode structure of the solar cell. The performance of a solar cell under illumination can be completely described by the current-voltage dependence. If we consider a typical current-voltage curve of a *pn*-junction diode in the dark and under illumination as shown in Figure 22 [28], we can characterize three parameters that give a complete description of the electrical behavior: *short-circuit current,* I_{SC}, *open-circuit voltage,* V_{OC}, and the *fill factor, FF*. These three parameters are sufficient to calculate the *energy conversion efficiency* η of the solar cell.

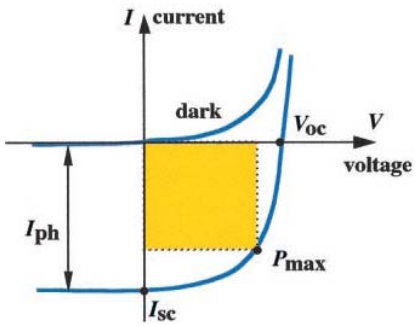


Figure 22. Current-voltage characteristics of a *pn*-junction solar cell. [28]

The short-circuit current I_{SC}, which obtained for $V_{OC} = 0$, is equal to the light-generated current, $I_{SC} = I_L$, if the series resistance R_S is zero. A finite series resistance R_S reduces the short-circuit current. The open-circuit voltage V_{OC}, which obtained for $I = 0$, is determined by the ratio I_L/I_S and thus by the absorption and light-generation processes and the efficiency with which the charge carriers reach the depletion region. In the ideal case where $I_{SR} = R_S = 0$ and $R_{sh} = \infty$, then:

$$V_{OC} = \frac{KT}{e} \ln\left\{\frac{I_L}{I_S} + 1\right\} \tag{23}$$

The performance of the solar cell is eventually determined by the fraction of the total power of incident light that can be converted into electrical power. Under illumination, the junction is forward biased and the external load resistance determines an operating point on the current-voltage curve. The electrical power output $P = IV$ is equal to the area of the rectangle. In general, the solar cell will be operated under conditions that give the maximum power output. The maximum possible area $P_{max} = V_{max}I_{max}$ for a given current-voltage curve determines the fill factor FF, which is defined by

$$FF = \frac{V_{\max} I_{\max}}{V_{OC} I_{SC}} \tag{24}$$

FF is larger the more "square-like" the current voltage curve is. Typically, it has a value of 0.7 to 0.9 for cells with a reasonable efficiency. The three parameters V_{OC}, I_{SC}, and FF are sufficient to calculate the energy-conversion efficiency η of the solar cell, which is defined by

$$\eta = \frac{V_{\max} I_{max}}{P_{in}} = \frac{FF \cdot V_{OC} \cdot I_{SC}}{P_{in}} \tag{25}$$

where P_{in} is the total power of the incident light. The essential material parameters that determine the efficiency of the solar cell are the lifetime and mobility of the minority charge carriers, and the surface recombination velocities. These parameters are not independent from each other and are controlled by physical processes.

The maximum current as a function of the band gap of the semiconductor is shown in Figure 23 [30] for the spectral distributions AM0 and AM1.5. The current increases with decreasing band gap, since more photons have enough energy to generate charge carriers.

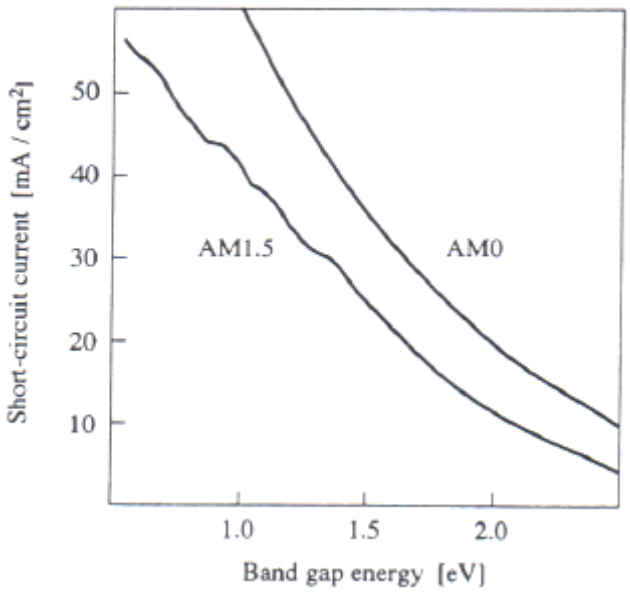


Figure 23. Short-circuit current as a function of the band gap energy for AM0 and AM1.5 spectral distributions. [30]

Saturation current I_S needs to be as small as possible for a maximum V_{oc}. With increasing E_g the saturation current decreases and the open-circuit voltage increases. This trend is opposite from that for I_{SC}; therefore, a maximum in the efficiency exists. Calculations for two different sun spectra are given in Figure 24 [22] and show that the optimum band gap occurs between 1.4 and 1.6 eV. The near-optimal efficiency for AM1.5 of 30% occurs at 1.5 eV for CdTe. There are two fundamental reasons for limited efficiency of a semiconductor solar cell based on an ideal *pn*-junction device. First, losses occur because

the energy of photons above E_g is wasted in the form of heat. Second, the output voltage is smaller than the maximum voltage which corresponds to the band gap energy E_g/e.

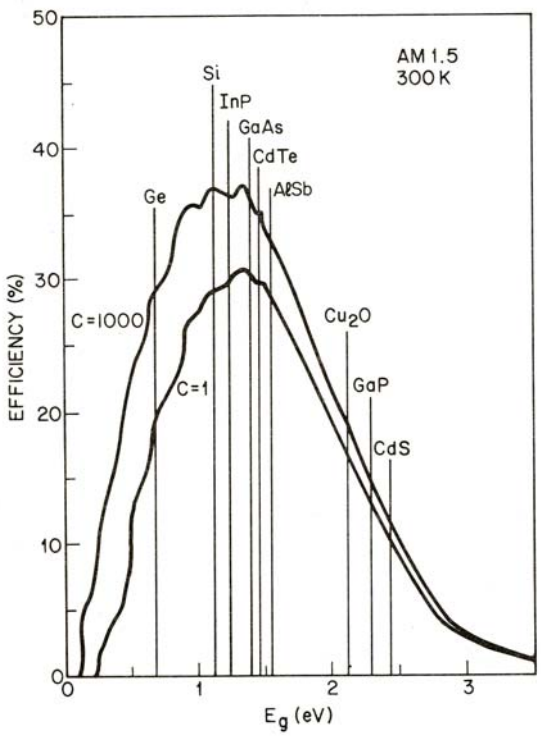


Figure 24. Ideal solar-cell efficiency at 300 °K for 1 sun and for 1000 sun concentration for AM1.5. [22]

2.6 Efficiency Losses

The important material parameters are the lifetime and mobility of the minority carriers in the bulk, and the recombination velocity at the front and back surfaces of the cell. Since the material parameters are closely linked to the technical design and the

fabrication of the solar cell, the actual device characteristics of the *pn* junction will be lower than its ideal values. The maximum limit for the photogenerated electric current density J_L is therefore given by the flux of photons with and energy $h\nu > E_{gap.}$ Thus, J_L decreases with increasing bandgap $E_{gap.}$ At the same time, the net energy transferred to each electron-hole pair increases, as it is equal to E_{gap}. There exists an "optimum" for E_{gap} for which a maximum of energy can be transferred from the incident sunlight to the totality of photogenerated electron-hole pairs. At this bandgap, roughly half of the incident solar energy is transferred. This limit will only be approached if optical losses due to reflection, shading by grid patterns, and so forth are minimized and if the semiconductor is thick enough to absorb all useful incident photons.

The maximum limit for J_{sc} is given by the photogenerated current density J_L. V_{oc} cannot exceed E_{gap}/q (q is the charge of an electron) and is lower due to recombination. At open-circuit conditions, all photogenerated carriers recombine within the solar cell. If recombination can be minimized, V_{oc} can more closely approach the limit (E_{gap}/q). From thermodynamic considerations of the balance between radiation and generation, one finds that recombination cannot be reduced below its radiative component, yielding a lower basic limit for V_{oc} [31].

Considering FF, Green [30] has calculated it as a function of V_{oc} by assuming that the *I-V* characteristics of a diode are, in an ideal case, an exponential function. The calculations show that the limit for FF increases with E_{gap}. The optimum value of E_{gap} for the total energy conversion efficiency (including charge separation) is ~1.5 eV, with a "limit" efficiency approaching 30% [32]. Figure 24 shows the ideal efficiency at an

optical concentration of 1000 suns. The ideal peak efficiency increases from 31% (C =1) to 37% (C = 1000). This increase is primarily caused by the increase of V_{oc}.

Efficient devices must have high conversion efficiency of solar photons and high collection efficiency of excited charge carriers. Thin film solar cells consist of several layers of different materials in thin film form. In general, the solar cell consists of a substrate, a transparent conduction oxide, a window layer, an absorber layer and a metal contact layer. Each of the component materials has different physical and chemical properties, and each affects the overall performance of the device. Equally important are the interfaces between the different layers. Each layer has a different crystal structure, microstructure, lattice constant, electron affinity; work function, thermal expansion coefficient, diffusion coefficient, chemical affinity and mobility, mechanical adhesion and mobility, the interfaces can cause stresses, defect and interface states, surface recombination centers, photon reflection/transmission/scattering, inter-diffusion and chemical changes.

2.6.1 Optical Losses

Losses in the light-generated current directly reduce the short-circuit current and the open-circuit voltage. The incident light cannot be fully utilized because of the finite reflectivity R. Most commonly used are antireflection (AR) coatings on the top surface of a material. Usually AR coatings are deposited as amorphous layers to suppress the light scattering at grain boundaries.

A further improvement is possible by the use of multiplayer coatings with different refractive indices. Another possibility for changing the reflectivity is by texturing the surface. This can be produced with particular etchants that preferentially attack inclined crystallographic planes so that pyramidal structures form. With the combination of both techniques, it is currently possible to keep the total reflectivity below 3% [1]. Optical losses also occur because of the finite thickness of the solar cell. In order to collect the major fraction of the sunlight inside the cell, a certain thickness of the material is required. The optical thickness of a semiconductor can be reduced by light trapping the light inside the crystal so that it is reflected several times between front and back surfaces before it is finally absorbed. This requires a mirror at the back side and textured surfaces which reflect the light at oblique angles. The incident sunlight is further reduced by the metal grid on the front side, which is necessary to make electrical contacts on the emitter side of the *pn* junction.

2.6.2 Recombination Losses

A fraction of the charge carriers is always generated far away from the junction, and some losses occur because minority carriers recombine before they can diffuse to the device terminals. Several recombination mechanisms can contribute to the minority carrier lifetime. Other important recombination centers are the surfaces, dislocations, gain boundaries in polycrystalline semiconductors, and interfaces in heterostructure solar cells. The recombination at the surface and in the bulk are also the fundamental processes that determine V_{OC}. The recombination current yields and increased saturation current,

which reduces the open-circuit voltage. The recombination processes in the entire cell should be minimized.

2.6.3 Series and Shunt Resistance

The current-voltage characteristics of the *pn* junction are further modified because of a series R_s and shunt R_{sh} resistance associated with the solar cell. The origin of the series resistance is the bulk resistance of the semiconductor and the resistance of the contacts and interconnections. The shunt resistance can be caused by extended lattice defects in the depleted region or leakage currents around the edges of the cell. Extended defects are dislocations, grain boundaries, and large precipitates. Plots for various combinations of the series and shunt resistance in Figure 25 [22] show that essentially the shape of the current-voltage characteristics and the fill factor FF changed. A shunt resistance as low as 100Ω does not significantly change the power output of the devices, it can be seen that a small series resistance of only 5Ω reduces the total efficiency by 30% [1].

2.6.4 Temperature Effects

A considerable fraction of the incident light is transformed into heat and the operating temperature of a solar cell can vary over a wide range. The temperature dependent material parameters are the band gap energy, which usually decreases, and the minority carrier lifetime, which generally increases, with increasing temperature. This

will increase the light generated current and thus I_{SC} slightly due to the increased light absorption and the increase in minority-carrier diffusion length. The open-circuit voltage will more rapidly decrease because of the exponential dependence of the saturation current on the temperature, and correspondingly the fill factor will degrade. The overall temperature effect causes a reduction of the efficiency as the temperature increases.

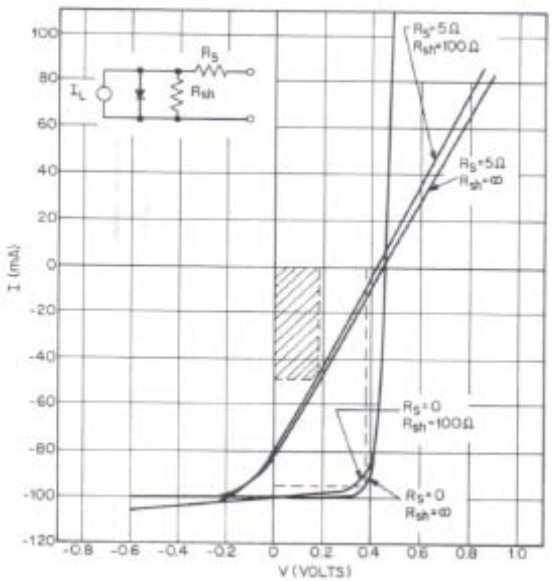


Figure 25. Theoretical I-V characteristics for various solar cells that include series and shunt resistances. [22]

Chapter 3

Experimental Methods

Several of the crystal growth and thin-film deposition techniques are carried out at high temperatures. It is important for the determination of the stoichiometry of the compounds to control the vapor pressure of the components at these temperatures. The microstructure of the films is mainly determined by the substrate temperature, the lattice match of the compound, the substrate properties, the process direction (substrate versus superstrate configurations), and the growth rate and pressure during deposition of the films. The electronic behavior of the films may also vary considerably with deposition conditions.

The CdTe solar cells can be grown in both substrate and superstrate configuration. All thin CdTe/CdS solar cells are of the substrate configuration shown in Figure 26. The basic device structure of the substrate cells studied is: stainless steel foil (SS) - SS/Mo/CdTe/CdS/ITO-based front transparent contact. Deposition techniques used for different layers include: rf-sputtering, close spaced sublimation (CSS), and thermal evaporation. Additional materials studied as the back contact to *p-type* CdTe include: ZnTe, Sb_2Te_3, Cu_2Te, Cu, and Au. Additional flexible foil substrates studied include: tungsten, tantalum, and molybdenum. Detailed device fabrication and characterization follows.

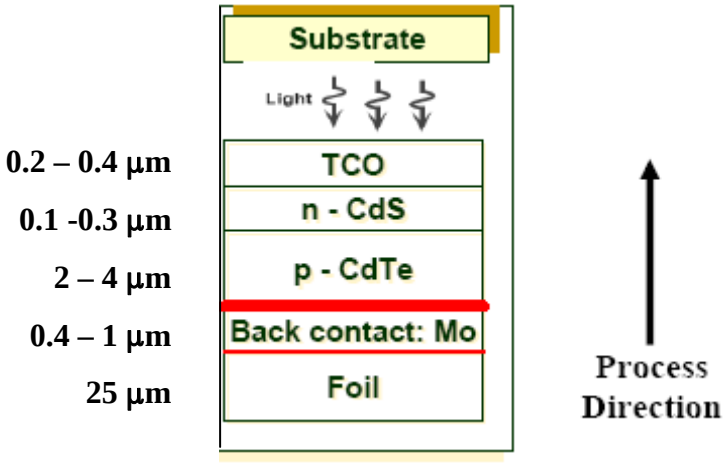


Figure 26. The CdTe thin film solar cell substrate configuration.

3.1 Substrate Preparation and Pretreatment

Different substrates have different influences on the film microstructure, growth of the layers, and the device characteristics. The substrate should withstand high temperatures experienced during the cell fabrication process. In addition, elemental impurities from the substrate must not diffuse into the layers of the solar cell device structure during high temperature processing. The substrate is a passive component in the device and is required to be mechanically stable, matching thermal expansion coefficient with deposited layers during the device fabrication.

The substrate selected is a stainless steel foil because of its commercial availability, low cost and ability to withstand relatively high temperature processing. Flexible stainless steel foil substrates are suitable for roll-to-roll deposition. The adhesion of CdTe solar cells on foil substrates with respect to substrate pretreatment on the

stainless steel foils. The Ar RF plasma treatment was also investigated and resulted in no significant improvements in adhesion.

The foil substrate surfaces exposed to air are covered by and absorbed hydrocarbon contamination layer as a result of the manufacturing process, surface preparation, and contact with the atmosphere. As a result, prior to solar cell fabrication, substrates were cleaned by ultrasonic solvent clean of three successive 30 minute rinses in acetone, methanol, and deionised (DI) water. Substrates were given a final rinse in DI water and dried with a nitrogen gas.

3.2 Solar Cell Device Fabrication

3.2.1 Back Contact: Molybdenum (Mo)

For polycrystalline CdTe solar cells, the back contact is applied to the *p-type* semiconductor. To form an ohmic contact, the metal used for the contact should have a work function greater than that of *p-type* CdTe, 5.7 eV. This aligns the metal Fermi level with the upper valence band edge. There are no low cost metals available with the appropriate higher work function to form the ohmic contact on CdTe. Use of an insufficient metal could result in the formation of a Schottky barrier at the back contact. As an alternative approach, pseudo-ohmic contacts are being researched for CdTe devices. With this approach, a highly doped semiconductor buffer layer is first deposited on a metal film followed by the deposition of the CdTe layer.

In superstrate configuration, commonly used buffer layer/metallization combinations are Cu/Au [33, 34], Cu/graphite [35] or graphite pastes doped with Hg and Cu [36], ZnTe doped with Cu [37-39] and Au or Ni metallization, Cu/Mo [40]. Alternatively, Cu free back contacts such as Ni:P, ZnTe [41], Au [42] or Sb_2Te_3/Ni [43] contacts have also been investigated [44]. A PVD deposited Sb buffer layer with Mo metallization has yielded high efficiency and low degradation in long-term performance [43]. Best cell stabilities have been achieved with RF sputtered Sb_2Te_3 buffer layer with Mo metallization as introduced by N. Romeo et al. [45]. Long term stability data for different buffer layer/metallization combinations obtained by light soaking at elevated temperatures are shown in Figure 27 [44].

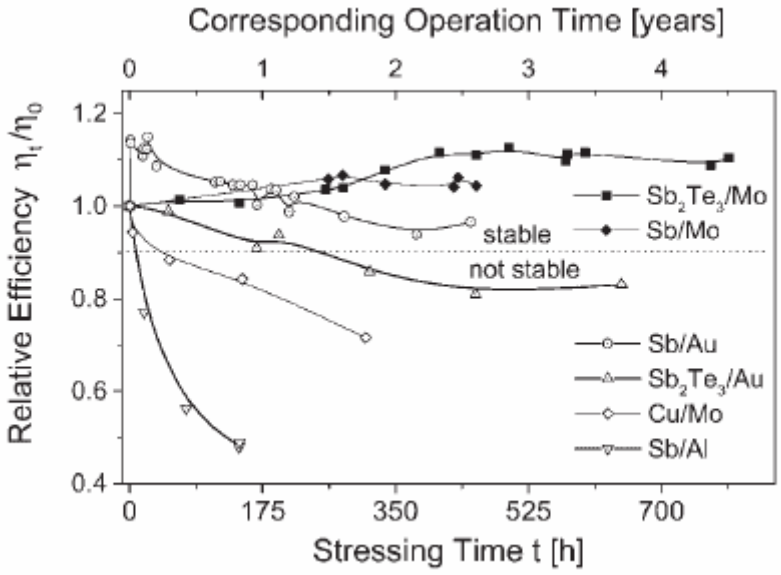


Figure 27. Stability of CdTe cells with different back contacts on comparable absorbers. Cells with Cu-based contacts show fast degradation while cells with Sb_2Te_3 /Mo are stable.[44]

Mo was selected as a metal electrode to be deposited on foil substrates. Deposition parameters affect Mo morphology and film resistivity. The baseline back contact structure consists of a Mo bi-layer (high-ρ/low-ρ), deposited by rf sputtering in an Ar ambient, at room temperature; the thickness and resistivity of the bi-layer were approximately 0.5 μm and 1.74×10^{-4} Ω·cm respectively. The first Mo layer deposited using low power (150 watts) and high Ar pressure (10 mTorr) resulted in grains that were not densely packed, highly resistive and tensile. The second Mo layer deposited using high power (400 watts) and low Ar pressure (4 mTorr) resulted in grains that were densely packed, least resistive and compressive. The high-ρ(tensile)/low-ρ(compressive) Mo bi-layer promotes adhesion of the device structure to the foil substrate, also acts as a diffusion barrier layer, and a roughness leveling layer. Other materials were investigated as back contacts including: ZnTe, Sb_2Te_3, Mo_2C, Cu_2Te, Cu and Au. Results will be presented in section 4.2, "Development of Back Contacts".

3.2.2 Absorber: Cadmium Telluride (CdTe)

CdTe can be deposited using several different deposition methods. When CdTe is deposited onto substrates above 449°C, it condenses stoichiometrically as the stable phase in this regime [46]. The CdTe phase diagram is shown in Figure 28, is characterized by a congruently melting intermediate phase, α-CdTe, which forms at 50 atomic percent Te. The high liquidus temperature of 1099°C at 50 atomic percent Te, results from a strong ionic binding between Cd and Te atoms. In the cases of high temperature depositions, the films are deposited with Cd deficiencies, resulting in

material property of *p-type* conductivity. In the Te-rich limit CdTe is *p-type* conducting since the Fermi energy is pinned closer to the valence band maximum. Because of the high ionicity (72%) of CdTe, the crystallite formed is well passivated and strong chemical bonding (5.75 eV) results in high chemical and thermal stability [47].

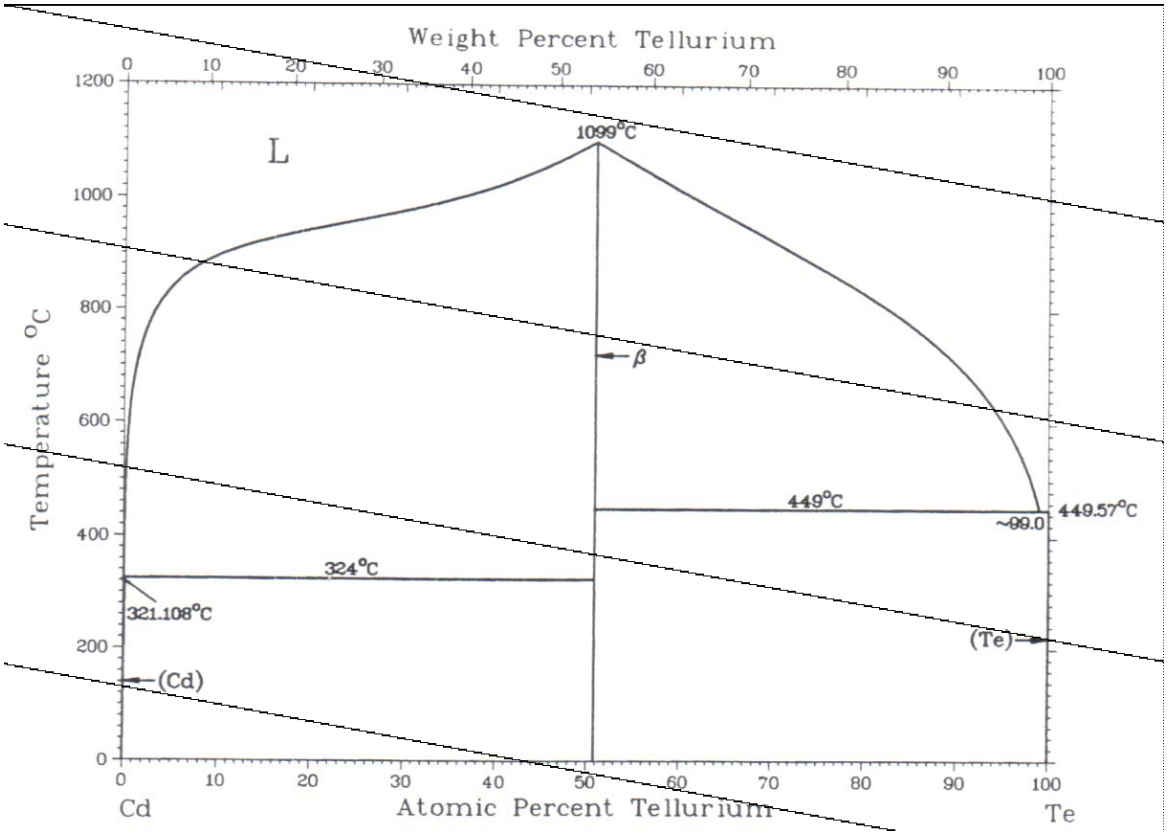


Figure 28. CdTe phase diagram. [48]

The most common CdTe solar cell structure is a *p*-CdTe/*n*-CdS heterojunction. The standard processes used to deposit CdTe thin films are:

1. Close spaced sublimation (CSS)
2. Chemical spraying (CS)
3. Screen printing (SP)

4. Chemical vapor deposition (CVD)
5. Sputtering
6. Electro-deposition (ED)
7. Physical vapor deposition (PVD)

The highest reported efficiencies for CdTe laboratory devices have been achieved with the close spaced sublimation (CSS) process [36, 49-51]. A thin film of CdTe with thickness of approximately 2 μm will absorb about 100% of the incident photons, due to its absorption coefficient of 10^5 cm^{-1} [47].

There is a 10% lattice mismatch at the CdTe/CdS interface that results in dislocations and can impact the grain size. The CdTe layers grown by high temperature (~550°C) CSS processes have grain sizes equivalent to the CdS grain size at the interface, but develop into much larger grains of several microns in diameter near the CdTe top surface. Figure 29 show the effects of deposition process on grain size, and that small CdTe grains re-crystallize into large grains, after a heat treatment process. However, large CdTe grains do not re-crystallize.

The CdTe films in the flexible substrate configuration were deposited by CSS at substrate temperatures in the 400-650°C range; the CdTe and CdS films were in some instances deposited in-situ. The thickness of the CdTe films ranged from 2-4 μm. Devices with reduced CdTe layer thickness were investigated and performances were comparable to those of thicker CdTe layers. Results are reported in section 4.3, "Optical Absorption and Transmission".

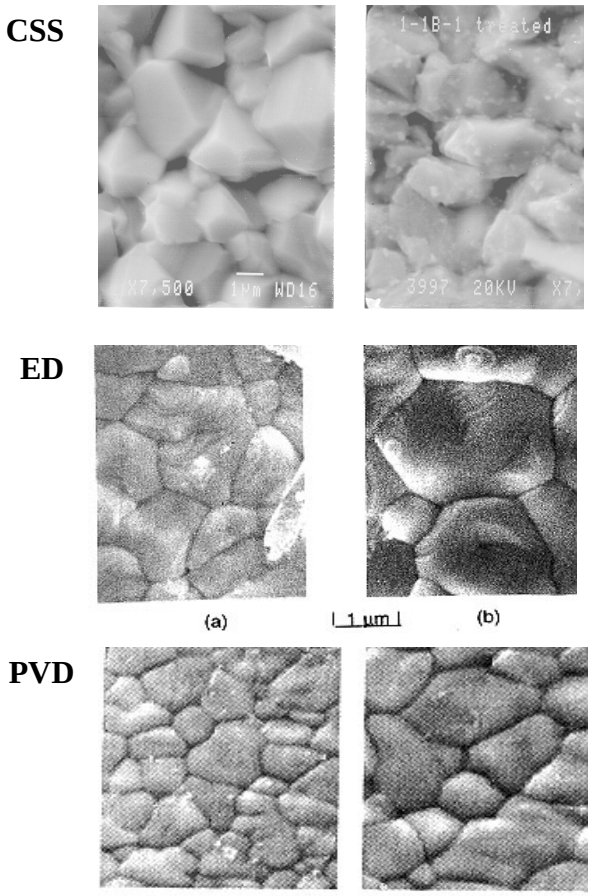


Figure 29. CdTe grain size (a) as grown, and (b) re-crystallized after heat treatment process.

3.2.3 Window: Cadmium Sulfide (CdS)

The primary function of a window layer in a heterojunction is to form a junction with the absorber layer while admitting a maximum amount of light to the junction region and absorber layer. For high optical throughput with minimal resistive loss the bandgap of the window layer should be as high as possible and as thin as possible to maintain low

series resistance. The optical transmission, thickness and film resistivity can be optimized to improve the solar cell device output.

The most effective heterojunction partner for CdTe, also referred to as a window layer, is cadmium sulfide (CdS). A key reason for the high quality and efficient CdTe/CdS junction is the fact that CdTe and CdS are miscible, and a reaction between these two materials during the cell fabrication process leads to the formation of an interfacial layer of $CdS_{1-x}Te_x$ [52]. The formation of this layer is believed to be responsible for lowering the interfacial defect density resulting in high efficiency devices [7]. The $CdS_{1-x}Te_x$ can form during a post deposition heat treatment of the of the CdTe/CdS structure in the presence of $CdCl_2$. The enhanced conversion efficiencies achieved as a result of the use of this heat treatment are primarily due to: (i) the formation of the interfacial layer, (ii) recrystallization and grain growth in the CdTe film, (iii) defect passivation/carrier lifetime improvement in the absorber [53].

Layers of *n*-conducting CdS are easily grown by various deposition methods including chemical bath deposition (CBD) as well as physical vapor deposition (PVD). CdS grows under most deposition conditions in a stable stoichiometric phase, α-CdS, which has the hexagonal wurtzite structure. The CdS phase diagram is shown in Figure 30. Under high pressure growth conditions or in thin films, CdS may be found in the cubic, metastable zincblende structure. High vacuum evaporation grown CdS films exhibit sub-micron sized, columnar grains that grow with preferred orientation parallel to the substrate, shown in Figure 31, [44]. CdS remains the best heterojunction partner for CdTe, because high efficiency devices with reduced lattice mismatch can be fabricated by forming an interfacial $CdS_{1-x}Te_x$ alloy layer.

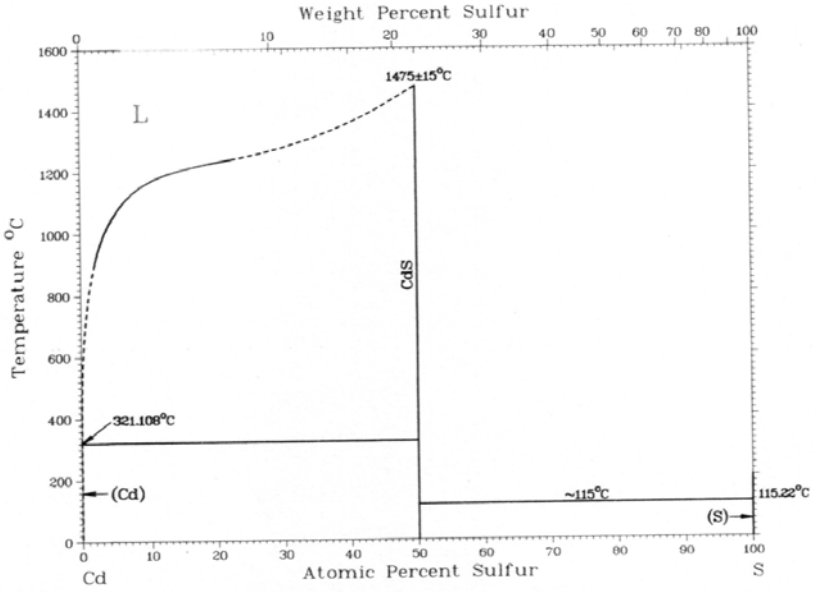


Figure 30. CdS phase diagram. [48]

The CdS films in the flexible substrate configuration were deposited by CSS at substrate temperatures in the 400-650°C range; the CdTe and CdS films were in some instances deposited in-situ. The thickness of the CdS films ranged from 0.1-0.3 μm.

Following the CdS deposition, all structures were subjected to a heat treatment in the presence of $CdCl_2$. The baseline $CdCl_2$ process was carried out by first depositing $CdCl_2$ onto the CdS surface by evaporation, and subsequently heat treating the structures at temperatures in the range of 380-425°C at atmospheric pressure in the presence of O_2.

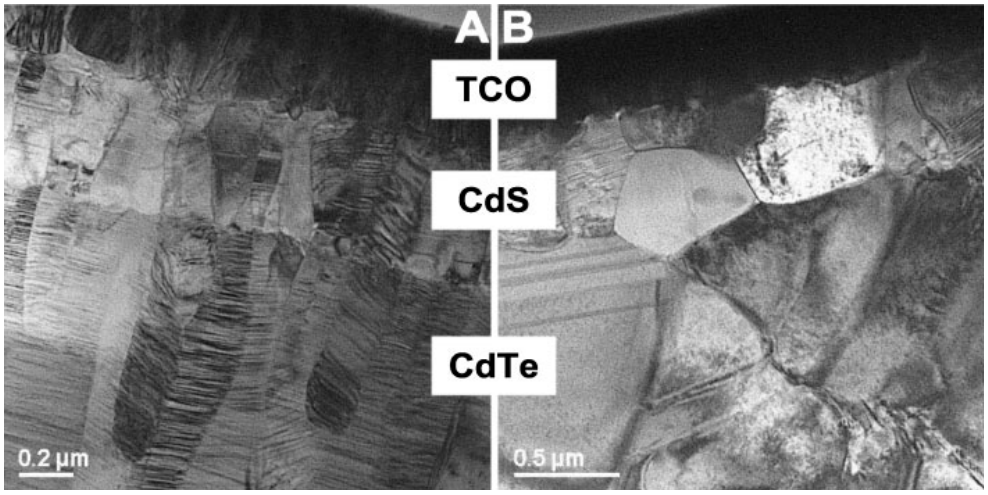


Figure 31. Characterization of CdTe and CdS layers. (A) TEM micrograph of the cross-section of a CdTe/CdS cell after deposition—both the columnar grain structure and the high density of twins on {111} plains in the CdTe and {0001} plains in the CdS layer are visible; (B) a sample area after $CdCl_2$ treatment—both, the CdTe and the CdS layers are characterized by grain growth (note the different scale bars), recovery and recrystallization; the CdTe/CdS interface exhibits grain coarsening [44].

3.2.4 Front Contact: Indium Tin Oxide (ITO)

A highly transparent and conducting oxide (TCO) layer with an electron affinity below 4.5 eV is required to form an ohmic contact and a good band alignment with the CdS. If the electron affinity of the TCO is higher than that of CdS, a blocking Schottky contact is formed. Transparent conducting oxides in general are *n-type* semiconductors with good electrical conductivity and high transparency in the visible spectrum. A low resistance contact to the device and transmission of most of the incident light to the

absorber layer is ensured. The conductivity of the TCO depends on the carrier concentration and mobility.

The most commonly used TCOs for CdTe solar cells, ITO, SnO_2:F, ZnO and their transmission spectra are shown in Figure 32. ITO front contacts are often sensitive to an annealing treatment, an increase of the electron affinity from around 4 to 5 eV, caused by oxidation or a post-deposition treatment, results in a blocking contact [54, 55]. They are often used in combination with a thin intrinsic SnO_x layer between the TCO and the CdS window layer maintaining a high voltage by preventing possible shunts through pinholes in the CdS [56]. Intrinsic (high resistivity) TCO facilitates the use of a thinner CdS layer for reducing photon absorption losses for wavelengths smaller than 500 nm [44]. The use of a bi-layer transparent contact, one that consists of a low/high resistivity (ρ) stack of transparent films has been found to effectively minimize efficiency losses resulting from the use of thin CdS films [57, 58]. Table 2 lists typical values of resistivity and transmission in the visible region for various TCOs of interest for photovoltaic application [59, 60].

The baseline transparent front contact structure in the flexible substrate configuration consists of a SnO_2/ITO bi-layer, deposited rf sputtering in an Ar ambient, at a pressure of 2-4 mTorr, and at substrate temperatures in the 200-300°C range; the thickness of the ITO films ranged from 0.2-0.3 μm.

Table 2. Typical resistivity and transmission (in the visible) for various TCO materials investigated for thin film solar cells. [59, 60].

Material	Resistivity (Ω cm)	Transparency (%)
SnO_2	8×10^{-4}	80
In_2O_3:Sn (ITO)	2×10^{-4}	>80
In_2O_3:Ga (IGO)	2×10^{-4}	85
In_2O_3:F	$2{\cdot}5 \times 10^{-4}$	85
Cd_2SnO_4 (CTO)	2×10^{-4}	85
Zn_2SnO_4 (ZTO)	10^{-2}	90
ZnO:In	8×10^{-4}	85

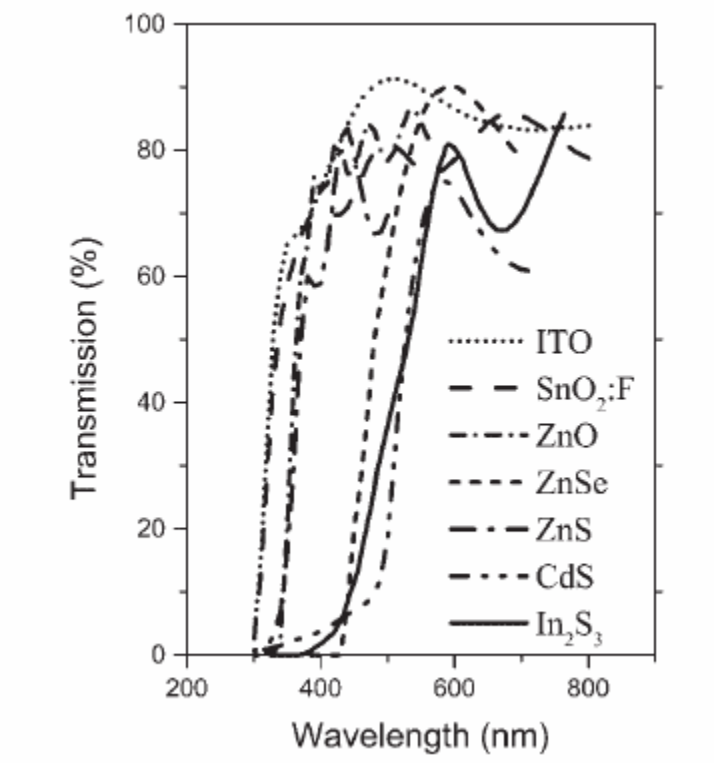


Figure 32. Optical transmission of different front contacts and buffer layers.

3.3 Solar Cell Device Characterization

Solar cells were characterized using standard solar cell techniques such as dark and light J-V, and spectral response (SR) measurements. SEM, AFM, XRD, EDS and optical transmission measurements were performed to study the structure and morphology of the films and devices.

Chapter 4

Discussion and Results

4.1 Mechanical Properties and Adhesion

4.1.1 Introduction

Excellent adhesion is required of a CdTe thin film solar cell device fabricated on a flexible foil substrate. Interlayer adhesion and cohesion can be a problem for both flexible substrate CdTe solar cells [14] and thin-film module reliability [61]. Film delamination can result in solar cell performance degradation and device failure. The primary objective of this work is to study the device materials and interfaces, and their response to stress; and to develop a process that achieves strong adhesion of the solar cell structure onto flexible metallic foils. This study is being performed as part of the development a novel flexible substrate CdTe solar cell, and the development of an efficient, pseudo-ohmic back contact. The basic device structure of substrate cells being studied is: SS/Mo/CdTe/CdS/ITO-based front transparent contact. Substrate foils evaluated include: SS316, SS430, Tantalum, Molybdenum, and Tungsten. Adhesion is being studied by analysis of the foil substrate effects, surface roughness, stress, microstructure of Molybdenum, and the coefficient of thermal expansion mismatch

between the substrate and the film layers. A major challenge associated with the flexible substrate CdTe cell is achieving strong adhesion of the solar cell structure onto the metallic foil. Substrate characteristics such as the coefficient of thermal expansion, surface roughness and substrate composition, strongly influence growth and properties of the following layers. Adhesion failure, flaking, delamination, buckling, and contamination by diffusion of impurities from the substrate may occur with some substrates, resulting in degradation of the solar cell device performance or complete device failure.

4.1.2 Experimental Details and Results

Flexible foil substrates (stainless steel SS316, SS430, tantalum, molybdenum and tungsten) were cleaned in an ultrasonic bath with acetone, methanol and deionised water. A metal electrode (Molybdenum) was deposited by rf sputtering on the stainless steel substrates. The CdTe/CdS layers were deposited by close spaced sublimation (CSS). Substrate temperatures ranged from 300 to 550°C. The solar cell structures were heat treated in the presence of $CdCl_2$ for 20 minutes at temperatures ranging from 380-425°C, followed by the deposition of an ITO-based front transparent contact by rf-sputtering. SEM, AFM and XRD measurements were performed to study the structure and morphology of the devices. ASTM D3359-08 tape tests, light I-V characteristics and spectral response measurements were used to study the effect of various processing conditions on adhesion and of the solar cells devices fabricated.

4.1.2.1 Substrate Effect on Adhesion and Morphology

The adhesion of CdTe solar cells on foil substrates with respect to substrate pretreatment of the stainless steel foils was investigated. The Ar^+ RF plasma treatment was also investigated and resulted in no significant improvements in adhesion. The foil substrate surfaces exposed to air are covered by an adsorbed hydrocarbon contamination layer as a result of the manufacturing process, surface preparation, and contact with the atmosphere. Substrates were cleaned by ultrasonic solvent clean of successive rinses in acetone, methanol and deionised water.

The initial layer of Mo in the Mo bi-layer acts as a diffusion barrier on the SS316 and SS430 substrates, promotes adhesion by reducing stress as the tensile layer before the compressive layer of Mo, and helps to smooth the rough surface of the substrate. A smooth substrate surface is required for two reasons [63]. First, abrupt changes in the surface topography such as spikes or cavities may lead to shunts between the front and back contact, and degrade adhesion of the solar to the foil substrate. Second, the deposition of impurity diffusion barriers or buffer layers may be easier and more successful on a smooth substrate. AFM images of a SS316 foil substrate before and after Mo deposition are shown in Figure 33, where the surface roughness of the SS foil substrate is decreased 30% after the Mo deposition.

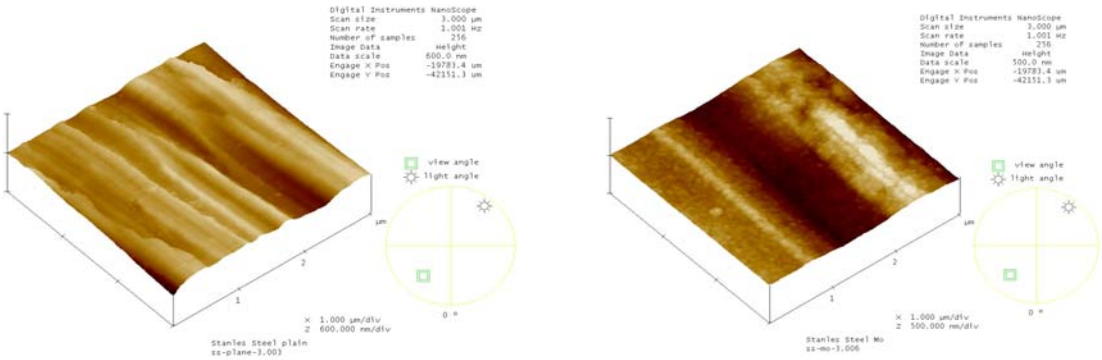


Figure 33. AFM images of SS316 foil substrate surface before and after Mo deposition. Before Mo, R_A=19nm (left), and after Mo, R_A=13nm (right). After the Mo deposition, the spikes and cavities are leveled out and surfaced roughness is decreased 30%.

4.1.2.2 Coefficient of Thermal Expansion Mismatch

The coefficient of thermal expansion (CTE) of the substrate must lie in the range of the CTE of the CdTe solar cell, otherwise adhesion problems can occur as a result of thermal expansion mismatch, as shown in Table 3. The effect of temperature on the observed results can be attributed to the differences in the coefficient of thermal expansion (CTE) of the various films result in a compressive film stress in the device structure. Use of an intermediate adhesion layer with a similar CTE and an alternate substrate with a smaller CTE can promote adhesion and is being studied.

Table 3. CTE, surface roughness and microstructure of foil substrates.

Substrate Material	**CTE (x 10^{-6}/°K)**	**ΔCTE (x 10^{-6}/°K)**	**Roughness R_A (nm)**	**Lattice Parameter (Å) Crystal Structure**
SS 316	16.5	10.6	19	3.5920 Cubic
SS 430	10.5	4.6	3	2.8839 Cubic
Ta	6.48	0.58	23	3.3058 Cubic
Mo	5.04	- 0.86	10	3.1472 Cubic
W	4.5	- 1.4	6	3.1648 Cubic

Substrate roughness strongly influences growth, crystal orientation and other properties of subsequent layers. Grain boundaries, defects, size, orientation and packing density directly impacts the overall solar cell device performance. CdTe solar cell devices were fabricated on three different substrates (tantalum, molybdenum and tungsten), using the same deposition conditions. The substrate affect on grain morphology is shown in Figure 34. Results of the ASTM D3359-08 tape test shows that flaking at the edges increases from W to Mo, and delamination within the squares increases from Mo to Ta, as the CTE increases within these three foils, as shown in Figure 35. The crystallographic orientation of the thin films on the three different substrates was investigated with X-ray diffraction. Figure 36 shows the XRD patterns of the films on the different foils. Each pattern exhibits a CdTe (111) orientation, with the highest (111) intensity exhibited on the Mo foil and lowest (111) intensity on the W foil.

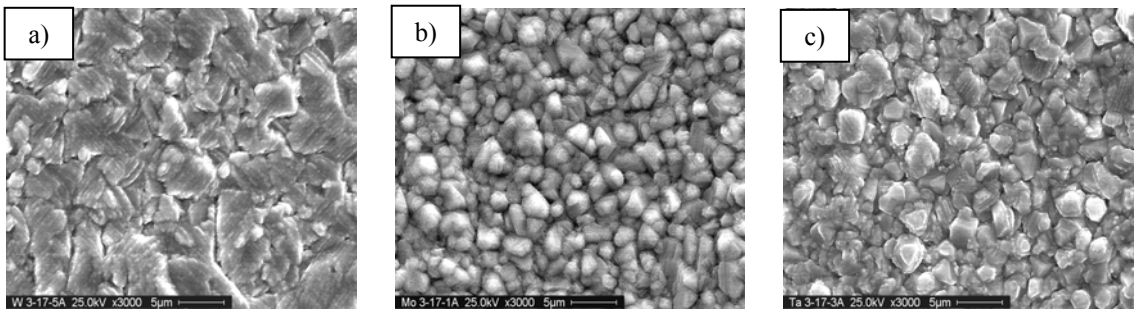


Figure 34. Substrate and surface roughness effect on CdTe solar cell morphology. SEM images of CdTe grains on a) W substrate, b) Mo substrate, and c) Ta substrate.

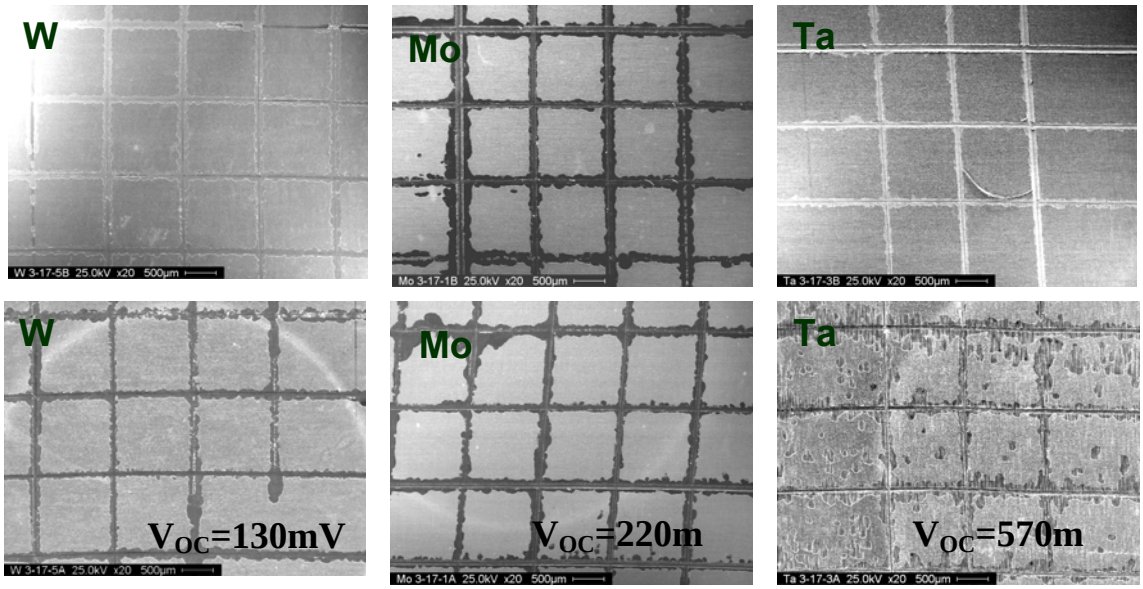


Figure 35. ASTMD3359-08 tape test results. CdTe solar cells were fabricated on three different substrates: W, Mo and Ta. The top row shows images of the as-deposited cells. The bottom row shows images of the cells after the $CdCl_2$ heat treatment. CTE mismatch minimization promotes adhesion and device performance for as-deposited films. The $CdCl_2$ chemical treatment increases flaking and delamination and requires optimization. The foil with the smallest mismatch, Ta, has the best solar cell device performance.

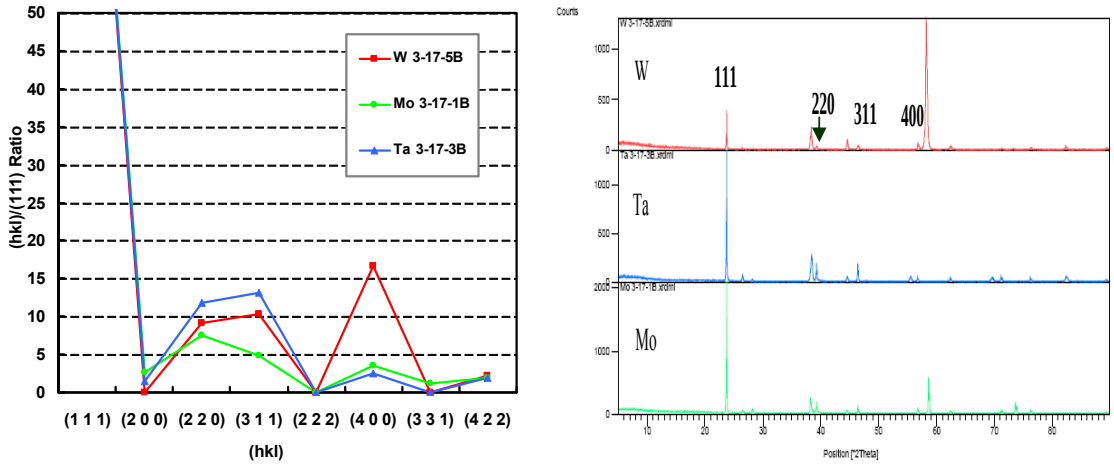


Figure 36. XRD patterns of CdTe thin films. Films deposited on the three different foil substrates, all exhibiting the CdTe (111) preferred orientation.

4.1.2.3 Molybdenum Bi-layer

Mo was selected as a metal electrode to be deposited on foil substrates. Deposition parameters affect Mo morphology and film resistivity. The film deposited using high power and low Ar pressure was densely packed, least resistive and compressive. The film deposited using low power and high Ar pressure was not densely packed, most resistive and tensile. Results are shown in Figure 37 and data summarized in Table 4. Our devices use a high-ρ(tensile)/low-ρ(compressive) Mo bi-layer to promote adhesion, act as a diffusion barrier layer, and a roughness leveling layer. Results show the grain size of Mo on SS increases as both the deposition rate and the pressure decrease. The resistivity decreases as the deposition rate increases and the Ar pressure decreases, which is in good agreement with the work of others [64, 65].

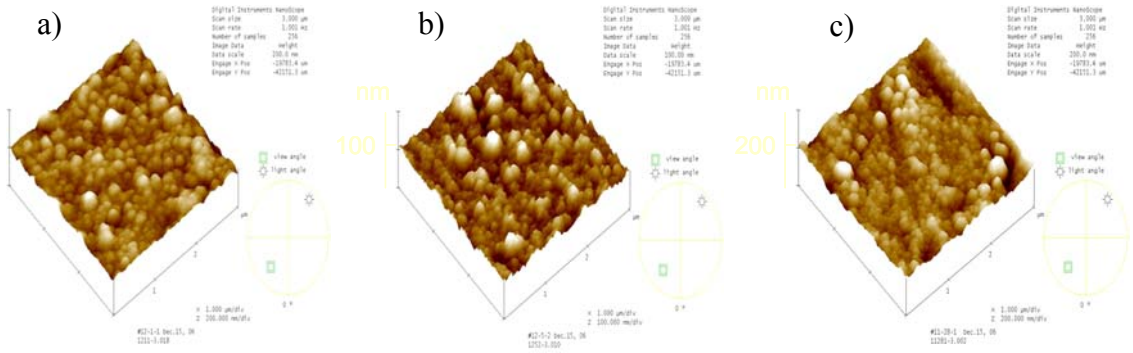


Figure 37. AFM images of Mo films on SS foil substrates. Illustrated are the effect of deposition parameters on film morphology and resistivity. Images a – c results and conditions are summarized in Table 4.

Table 4. Molybdenum morphology and resistivity data summary.

(a) Result of image (a)	
4 mTorr 10 Å/S	ρ=1.74x10^{-4} Ω•cm AFM 2D Grain size=223nm^2
Least resistive film Most densely packed film Compressive stress film	

b) Result of image (b)	
8 mTorr 6 Å/S	ρ=73.6x10^{-4} Ω•cm AFM 2D Grain size=309nm^2

c) Result of image (c)	
10 mTorr 2 Å/S	ρ=228x10^{-4} Ω•cm AFM 2D Grain size=910nm^2
Most resistive film Least densely packed film Tensile stress film	

4.1.2.4 Nanoindentation, Film Adhesion and Stress

Nanoindentation measurements were performed (with assistance from Dr. Kumar's research group and the USF Mechanical Engineering Department) with the ultimate objective to correlate the film mechanical properties to the deposition process; Young's Modulus and hardness data are shown in Figure 38 for two different samples of

Mo films on SS foils listed in Table 4. Although these should still be considered as preliminary, it appears that the film deposited at the fastest deposition rate has better mechanical properties (and the lowest resistivity). These results are encouraging and work to complete the sample matrix of Table 4 is needed. More meaningful adhesion measurements based on Nanoindentation are needed.

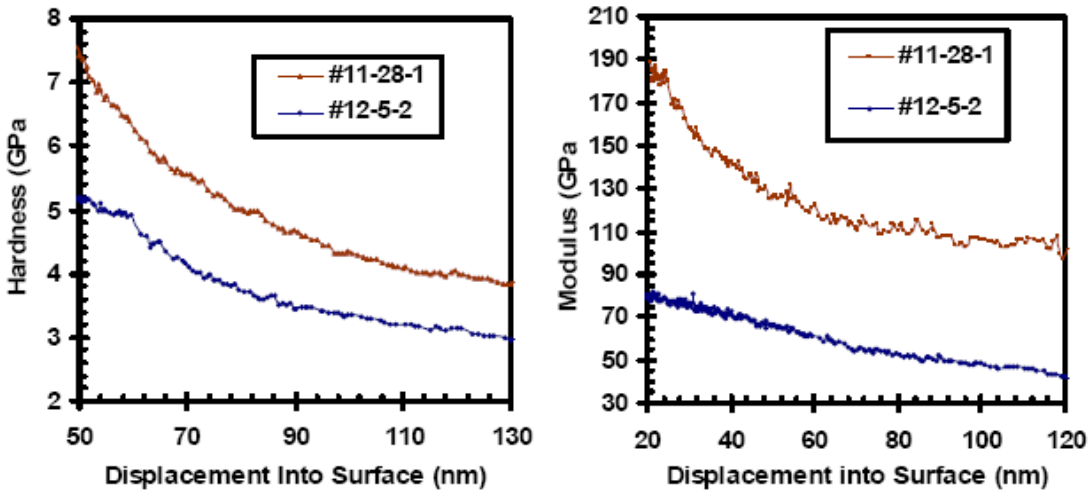


Figure 38. Hardness and Young's Modulus for two different samples (a and b) of Mo films on SS foils listed in Table 4.

While studying the effects of the Mo deposition process on the mechanical and adhesion characteristics of Mo films, it is important to recognize that the entire solar cell will be a multi-layer structure, to be completed by the sequential in-situ deposition to two possibly three semiconductors at high temperatures, which could affect the integrity of the foil/metal substrate. As already indicated above, solar cell structures are also being fabricated in parallel with the Mo adhesion studies. These have the following

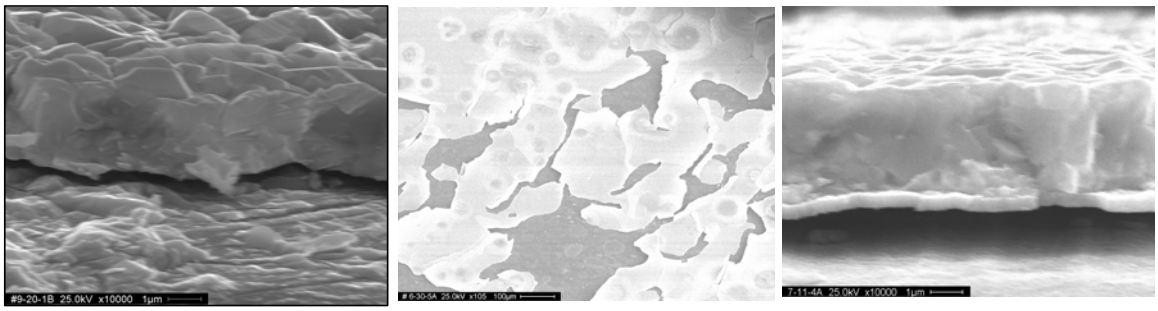
configuration: SS/Mo/ZnTe/CdTe/CdS, and are deposited on Mo films similar to sample (a) 11-28-1 (in Table 4). Semiconductor substrate deposition temperatures were in the range of 450-550°C (depending on the desired deposition rates); all deposition times being essentially identical and under one minute.

Figure 39 shows a photograph of three SS substrates (size 3.5 x 5.0 cm^2) with the multi-layer configuration described above; this image clearly demonstrates the varying degree of stress in the substrates (based on the variation in the curvature of the foil). Based on the limited number of structures fabricated to-date, there appears to be several parameters that affect the degree of curvature; two of them are: (a) the total film thickness and (b) the ultimate substrate temperature (and/or the exposure time at high temperatures). This work will continue in order to better understand stress and adhesion in these structures. The effect of temperature on the observed results can be attributed to the differences in the thermal expansion coefficients of the various films which varies by a factor of 2 to 3 among the various films and the SS foil substrate. Table 3 lists the CTE for the multi-layer stack of materials including the SS foil substrate and the mismatch in CTE which affect film stress and adhesion.

Figure 39. SS substrates coated with Mo and the solar cell semiconductors.

An interesting observation made to-date is the fact that based on simple tape-pull tests, the increased curvature in the substrates does not necessarily lead to poorer adhesion. Film delamination, flaking and debonding has been observed for both extreme and minimal curvature as shown in Figure 40. The adhesion of deposited films used in CdTe/CdS solar cell devices must be excellent both as-deposited, and after subsequent processing. Typically, for low values of adhesion, the electron shells of the adsorbed atoms remain intact, and these atoms are held to the surface by Van der Waals forces. These atoms are said to be physisorbed on the substrate. For high values of adhesion, sharing of electrons between the film and the substrate occurs, and the atoms are chemisorbed. Generally adhesion is greater the higher the absorption energy of the deposit and/or the higher the number of nucleation centers in the early growth stage of the film. Chemisorption due an intermediate-layer or "adhesion layer" formation that allows a continuous transition from one lattice to the other results in excellent adhesion.

Adhesion is also improved if intermetallic metal alloys are formed. In addition, adhesion is strongly affected by the cleanliness of the substrate, and the surface roughness of the substrate. Stress in a thin film is generally not sufficient to result in delamination, unless the film is extremely thick. More often, high stress results in the cracking of films.



(a) Delamination (b) Flaking (c) Debonding

Figure 40. Film (a) delamination, (b) flaking, and (c) debonding all as a result of stress, poor adhesion and CTE mismatch.

Typically, a thin film or multi-layer material bonded to a substrate supports some state of residual stress, which has a direct dependence on the film thickness. This residual stress can trigger significant undesirable consequences, including excessive deformation, fracture, delamination, microstructural changes in the materials, and device failure. This stress may be compressive or tensile. Compressively stressed films tend to expand parallel to the substrate surface, and buckle up on the substrate. Tensile stressed films tend to contract parallel to the substrate surface, and crack if their elastic limits are exceeded. Highly stressed films tend to exhibit poor adhesion, and the resistivity of stressed metallic films is higher than that of their annealed counterparts.

Growth or intrinsic stresses are dependent on:

1. the materials involved,
2. substrate temperature during deposition,
3. growth flux, and
4. growth deposition conditions.

The development of intrinsic stresses dependencies include the bonding of the deposit to the substrate, the mobility of adatoms on the film material itself, and the mobility of grain boundaries formed during growth. The final growth structure is typically metastable. Proposed mechanisms for stress generation during film material deposition include:

1. Surface and/or interface stress
2. Cluster coalescence to reduce surface area
3. Grain growth, or grain boundary area reduction
4. Vacancy annihilation
5. Grain boundary relaxation
6. Shrinkage of grain boundary voids
7. Incorporation of impurities
8. Phase transformations and precipitation
9. Moisture adsorption or desorption
10. Structural damage as result of sputtering or other energetic deposition process.

Typically, film-substrate material combinations grow in the Volmer-Weber (VW) mode which leads to a polycrystalline microstructure. Characteristic of this growth mode

is that deposited material gathers into discrete clusters or island on the substrate surface. Following the initial nucleation of islands of film material, successive stages typically include: island growth, island-to-island contact and coalescence into larger islands, establishment of large area contiguity, and filling in of the remaining gaps in the structure to form a continuous film. Once islands begin to interact to form grain boundaries, the process of grain coarsening can also contribute to structural evolution.

Nanoindentation measurements were performed and SEM images of indents of a solar cell on a SS foil are shown in Figure 41 and Load versus Displacement curves are shown in Figure 42.

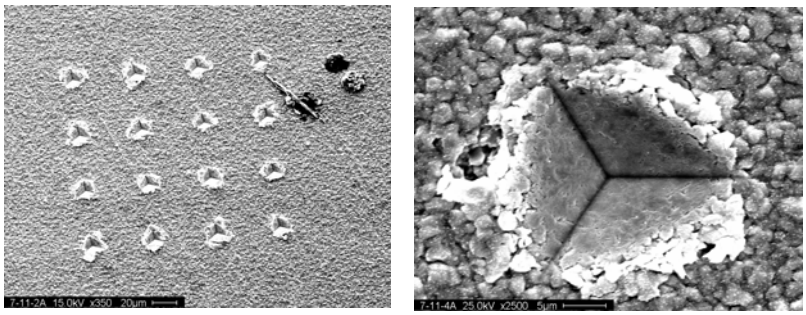


Figure 41. SEM images of nanoindentation data of a solar cell on a flexible foil substrate.

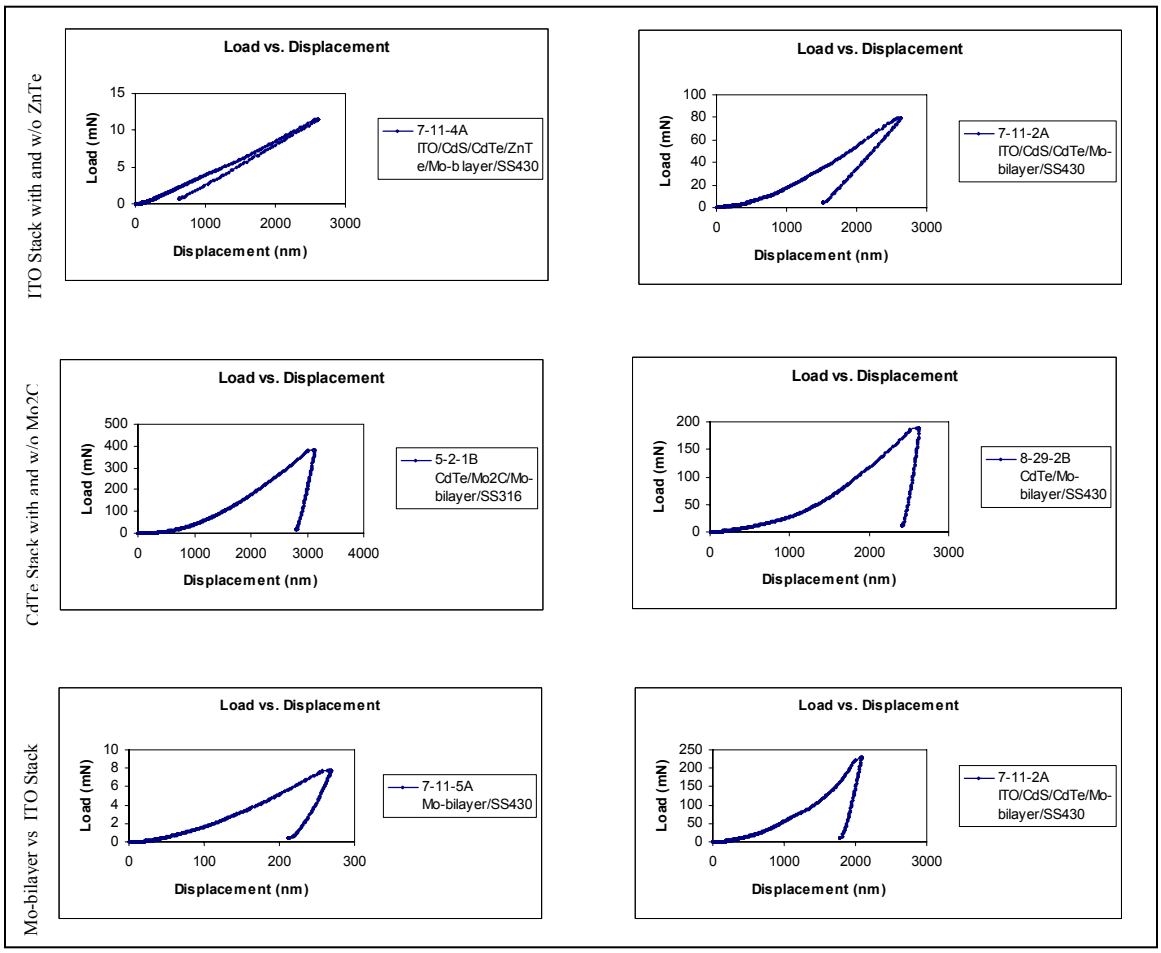


Figure 42. Load versus displacement curves of solar cells on flexible foil substrates.

4.1.3 Conclusions

Mismatch minimization of the substrate's CTE promotes adhesion and device performance of the CdTe solar cell device onto the flexible foil substrate (for as-deposited films). The effect of the $CdCl_2$ chemical treatment on the CdTe solar cell device increases flaking and delamination. Mo bi-layers reduce surface roughness and promote adhesion. Adhesion has significantly improved and studies continue with

minimizing CTE mismatch in the foil substrate, minimizing the surface roughness and optimizing the $CdCl_2$ treatment to promote adhesion of substrate CdTe thin film solar cells deposited on flexible foil substrates.

4.2 Development of Back Contacts

4.2.1 Introduction

An important issue associated with the fabrication of CdTe solar cells is the formation of a low resistance back contact of high stability. A number of materials are being investigated. The most promising approach used to-date is based on the use of an interfacial layer between the CdTe and a metal electrode, an approach that is believed to yield a pseudo-ohmic contact. The primary objective of this work is to investigate materials such as ZnTe and Sb_2Te_3 in the development of efficient back contacts for CdTe thin film solar cells deposited on flexible foil substrates in the substrate configuration. The ZnTe band alignment with CdTe is favorable for hole transport and can be easily doped p^+, and therefore easily contacted with a metal [66]. Extensive research on ZnTe doped with Cu has been done by Gessert et al. [67] and Tang et al. [37]. Copper-doped ZnTe makes a low resistance contact, although control of the Cu diffusing into the bulk CdTe and CdS is critical [37]. It has also been shown that if CdS is doped with Cu, this element need not be used for the formation of the back contact [68, 69]. Antimony telluride (Sb_2Te_3) deposited at low temperature is amorphous and resistive, but at higher temperatures, it crystallizes, and carrier densities increase with

substrate temperature to p ≈ 1 x 10^{20} cm^{-3} [70-72]. Romeo et al. [45, 62] first proposed the use of Sb_2Te_3 as an intermediate 'buffer' layer and demonstrated that the contact to CdTe can yield highly efficient and stable devices. Their 100 nm Sb_2Te_3 layers were deposited by sputtering at a substrate temperature of 300°C. There appears to be no evidence of Sb diffusion doping the CdTe. Formation of Sb_2Te_3 as a function of sputtering temperature has been investigated systematically [43]. Co-sputtering onto a low temperature substrate yields a mixed amorphous/crystalline deposit that converts to crystalline Sb_2Te_3 upon heating. Alternatively the crystalline Sb_2Te_3 can be formed by sputtering directly at temperatures above 200°C [73].

4.2.2 Experimental Details and Results

All thin CdTe/CdS solar cells discussed in this paper are of the substrate configuration shown in Figure 43. The substrates were flexible stainless steel foil, and prior to solar cell fabrication were ultrasonically solvent-cleaned in successive rinses of acetone, methanol and deionized water. The baseline metallization electrode structure consisted of a molybdenum (Mo) bi-layer, deposited by rf-sputtering at room temperature; the thickness of the Mo bi-layer was approximately 0.5 μm. Two different materials were investigated as potential back contact layers deposited between CdTe and Mo, ZnTe and Sb_2Te_3. The ZnTe layer was deposited by close-spaced sublimation (CSS); the thickness of the ZnTe ranged from 0.2-0.5 μm. Substrate temperatures ranged from 300-550°C. The Sb_2Te_3 films were deposited using two different approaches: (a)

deposited by evaporation from Sb_2Te_3 powder; the thickness of the Sb_2Te_3 films ranged from 0.1-0.2 μm, and substrate temperatures ranged from 150-450°C. (b) synthesized by depositing Te and Sb bi-layers and subsequently annealing them at temperatures ranging from 150-450°C, to form Sb_2Te_3. Both the CdTe and CdS layers were deposited by CSS at substrate temperatures in the 400-650°C range; the CdTe and CdS films were in some instances deposited in-situ. The solar cell structures were heat treated in the presence of $CdCl_2$ in O_2-containing ambient. The baseline transparent front contact consisted of ITO deposited by rf-sputtering at temperatures in the range of 200-300°C, and a thickness of 0.2-0.3 μm. Solar cells were characterized using standard solar cell techniques such as dark and light J-V, and spectral response (SR) measurements. SEM and XRD measurements were performed to study the structure and morphology of the films and devices.

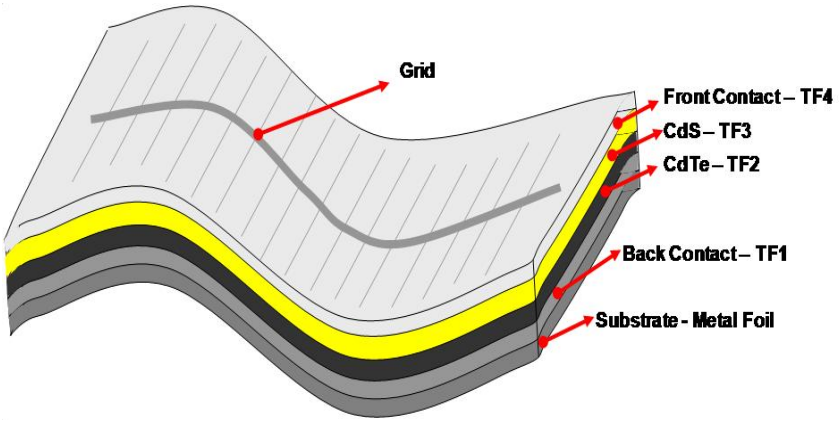


Figure 43. CdTe substrate device configuration.

4.2.2.1 CSS ZnTe

Zinc telluride has already been shown to be an effective back contact layer for the standard CdTe superstrate configuration [66] and can be easily deposited by CSS. The valence band position of ZnTe does not impede hole transport, while the conduction band can serve as an electron reflector which can have a positive impact on the collection of photo-generated carriers in CdTe. For this work no intentional dopant is introduced during the CSS deposition of ZnTe or during subsequent processing.

Figure 44 shows the effect of substrate temperature on the orientation of ZnTe films (XRD peak intensity ratio (hkl)/(111)). The data shown are for ZnTe films deposited at substrate temperatures in the range of 450-550 °C, and a source temperature of 630ºC. All films were found to exhibit preferential orientation along the (111) direction, with those deposited at the lowest temperature being the most highly oriented. This effect of substrate temperature on the orientation of ZnTe films has also been observed for CSS-CdTe [74, 75]. The ZnTe grain size for the films studied to-date is on the order of 0.1-0.3 μm, and the films are compact and consist of relatively uniform grains as shown in Figure 45 for a film deposited on a foil/Mo substrate. The resistivity of the CSS-ZnTe films was too high, and could not be measured using a four-point probe.

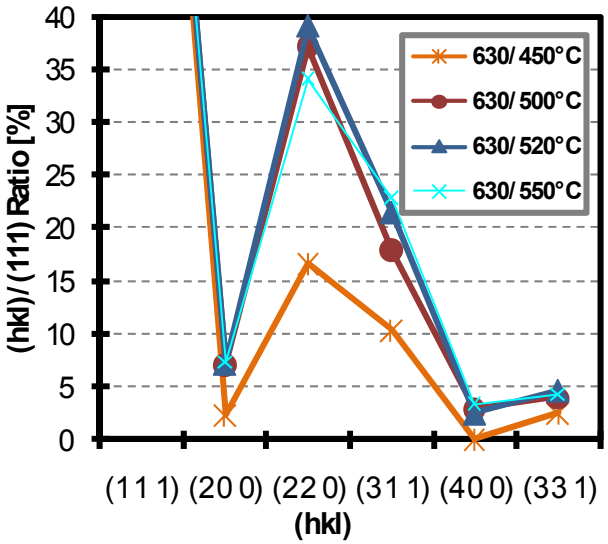


Figure 44. The effect of substrate temperature on the crystallographic orientation on ZnTe films deposited by CSS on Mo/foil substrate.

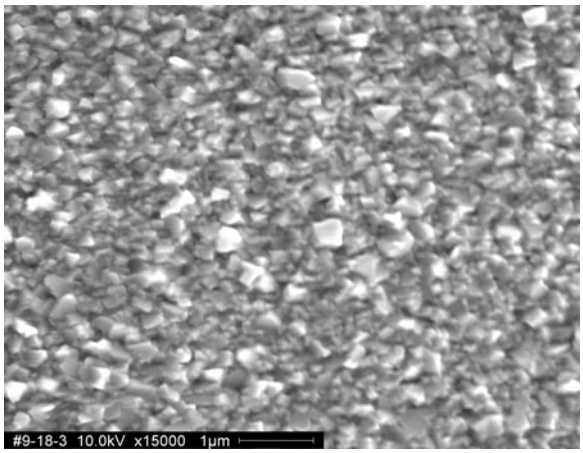


Figure 45. SEM image of a CSS-ZnTe film deposited on a foil/Mo substrate.

4.2.2.2 Sb_2Te_3 Films

Antimony telluride films were prepared using two different approaches: (a) direct evaporation from the Sb_2Te_3 compound, and (b) synthesis from annealed Sb/Te bi-layers.

4.2.2.2.1 Evaporation from Sb_2Te_3

Films prepared by direct evaporation from Sb_2Te_3 were deposited at temperatures in the range of 200-400°C. The XRD spectra for typical Sb_2Te_3 films deposited on glass substrates are shown in Figure 46; Table 5 lists the various diffraction peaks identified in the spectra of Figure 46. Identical results were obtained for films deposited on foil/Mo substrates (their XRD spectra are not shown here for clarity, since those contained additional peaks from Mo and the foil substrate). The spectra of the films deposited at the three highest temperatures were essentially identical with peaks having very similar intensities; all peaks have been identified to belong to the Sb_2Te_3 compound (see list in Table 5). The films deposited at the two lowest temperatures contain peaks that do not belong to the Sb_2Te_3 phase (shown in *italics* in Table 5). These have been assigned to Te.

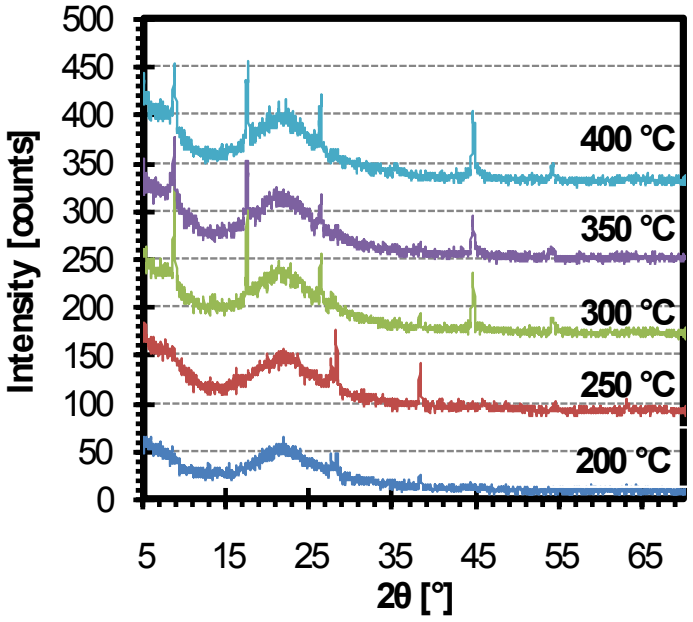


Figure 46. XRD spectra of Sb_2Te_3 films deposited by evaporation from Sb_2Te_3 on glass substrate.

The resistivity of the Sb_2Te_3 films deposited on glass was measured using a four-point probe and is shown in Figure 47 as a function of the deposition temperature. As the temperature is increased the resistivity decreases, with an apparent increase for the highest temperature; although this is well within the experimental error and must be verified with further studies. The highest and lowest resistivities measured are 5.4×10^{-5} and 8.0×10^{-6} Ω·m respectively. Attempts to deposit Sb_2Te_3 at higher temperatures were mostly unsuccessful due to re-evaporation of the compound.

Table 5. 2θ values and the corresponding (hkl) directions for the Sb_2Te_3 films. Reference Figure 46.

	2θ [º]				
	200 °C	**250 °C**	**300 °C**	**350 °C**	**400 °C**
(003)			8.689	8.6719	8.6976
(006)			17.4601	17.449	17.5237
(009)			26.3759	26.3609	26.3349
(101)	*27.6127*	*27.6049*			
(015)	28.2447	28.2094			
(1010)	38.3351	38.3261	38.2853	38.3635	
(0015)		45.8993	44.5778	44.6826	44.6595
(0018)		54.472	54.1933	54.0657	54.2542
(1019)		63.2481			

Assuming typical values for thin film carrier mobilities of the order of 10-20 $cm^2/V{\cdot}s$, the carrier density for the evaporated films shown above ranges from the mid 10^{19} to mid/high 10^{20} cm^{-3}. These results are consistent with Wang et al. [71] who found that for Sb_2Te_3, the mobility increases nearly five times from 0.7634 to 3.721 $cm^2/V{\cdot}s$, and the carrier density increases less than two times from 8.46 x 10^{19} to 1.50 x 10^{20} cm^{-3}. It indicates that the drop of electrical resistance is mostly contributed by the increase of mobility. The resistivities obtained here are significantly lower than those reported by Romeo et al. [76] for films deposited by sputtering at a substrate temperature of 300°C and a film thickness of 300 nm. Crystals of Sb_2Te_3 prepared from stoichiometric amounts of Sb and Te typically contain an overstoichiometric amount of Sb [72]. The excess of Sb is closely related with the concentration of native defects, notably the antisite defects, where Sb occupies the lattice site of Te. A single negative charge that such a defect carries is compensated by a positively charged hole, giving rise to a high background

hole carrier density on the order of 10^{20} cm^{-3} at room temperature, and resulting in a decrease in electrical resistivity of the Sb_2Te_3 films developed in this research.

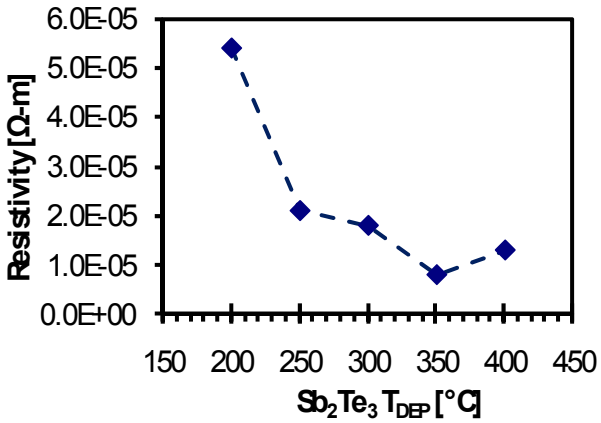


Figure 47. Resistivity of Sb_2Te_3 thin films deposited by evaporation at various substrate temperatures.

4.2.2.2.2 Synthesis of Sb_2Te_3 Films from Sb/Te Bi-layers

Antimony telluride films were also synthesized by annealing bi-layers of Te and Sb in order to ultimately be able to control the stoichiometry of the compound and incorporate excess Te or Sb. For this work the thicknesses of Te and Sb were calculated to yield a ratio of 3:2 in order to synthesize the Sb_2Te_3 compound. In some cases Te was deposited first followed by the deposition of Sb, and in others the sequence was reversed. The bi-layers were annealed at various temperatures in inert ambient.

Figure 48 shows XRD spectra for four Sb/Te films; these were deposited on Mo coated foil substrates and were annealed at 200 and 350ºC, with Te or Sb being deposited

first (the legend Sb/Te indicates that Sb was deposited first, and Te/Sb indicates that Te was deposited first). The films annealed at 350ºC contained the Sb_2Te_3 phase and exhibited very similar XRD spectra irrespective of the sequence of deposition of the elements. The films annealed at 200ºC with Sb deposited first did not show evidence of the Sb_2Te_3 being present; however, Sb_2Te_3 was found in the films where Te was deposited first. All films contained peaks associated with Te or Sb. The main Sb_2Te_3 peaks identified in the various films are marked in Figure 48 with "down" arrows. The unmarked peaks are associated with the elements or the substrate materials.

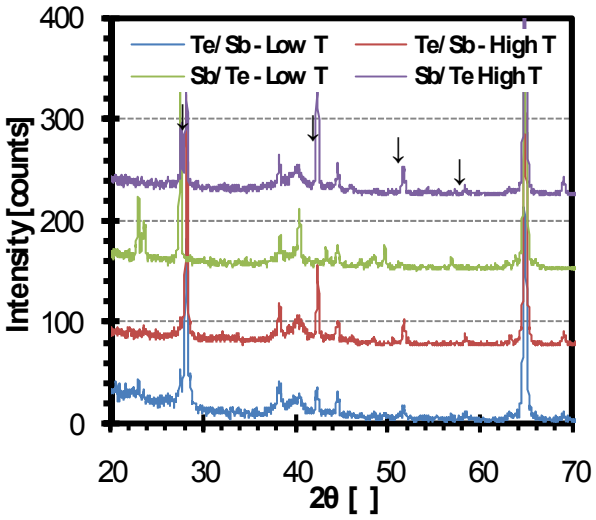


Figure 48. XRD spectra for Sb-Te films synthesized from Te/Sb bi-layers.

4.2.3 Conclusions

Two different materials are being investigated as back contact candidates for substrate CdTe thin film solar cells deposited on flexible foil substrates: ZnTe and Sb_2Te_3. Sb_2Te_3 films prepared by evaporation from the Sb_2Te_3 compound have been found to be superior to those synthesized by annealing of Te/Sb bi-layers which contained elemental phases; processing conditions for films synthesized by annealing of elemental bi-layers will have to be improved/optimized in order to produce single phase Sb_2Te_3. The Sb_2Te_3 resistivity was found to decrease with deposition temperature; the resistivity for films studied to date was found to be in the range $8.0x10^{-6}$ - $5.4x10^{-5}$ $\Omega \cdot m$. The decrease in resistivity of Sb_2Te_3 is attributed to an increase in carrier mobility. Solar cell results suggest that ZnTe is more suitable as a back contact material based on the highest V_{OC} obtained from ZnTe-contacted cells, even though this material was not intentionally doped (and exhibited high resistivity). This suggests that doping of ZnTe can result in significant improvements in the back contact characteristics and overall solar cell performance. All solar cells exhibited I-V characteristics with a significant roll-over in the 1^{st} quadrant suggesting the presence of a strong barrier at the back contact.

4.3 Optical Absorption and Transmission

4.3.1 Introduction

The efficiency of a CdS/CdTe solar cell is a key characteristic because it allows the device to be evaluated in comparison to other solar cells, and also, other energy conversion devices. The CdS/CdTe solar cell efficiency is the fraction of incident light energy converted to electrical energy. This conversion efficiency depends on both the semiconductor material properties and the device structure. This characteristic is dependent on the optical energy that is absorbed in the semiconductor and the excess electron-hole pairs (EHPs) generated that produce photocurrents.

Photogenerated EHPs far away from the depletion region are lost by recombination. It is important to have the minority carrier diffusion length L_e in *p*-CdTe as long as possible. At long wavelengths, around 0.7 μm, the absorption coefficient α of CdTe is 10^4 cm^{-1} and the absorption depth (1/α) is typically greater than 1 μm. The absorption coefficient is the relative number of photons absorbed per unit distance, expressed in terms of cm^{-1}. If the absorption coefficient is large, the photons are absorbed over a relatively short distance. The absorption coefficient in the semiconductor is a very strong function of photon energy and bandgap energy. Figure 49 shows the absorption coefficient α plotted as a function of wavelength for several semiconductor materials [27]. The absorption coefficient increases very rapidly for $hv > E_g$.

To efficiently capture these long wavelength photons, the thickness of *p*-CdTe plays a crucial role. This study looks at the optical absorption and transmission effects

based on the thickness of *p*-CdTe, and the overall effects on device performance and efficiency. To determine the optimum thickness of CdTe that will absorb 90% of the incident photon energy, we will use the relation,

$$I_v(x) = I_{v0}e^{-\alpha x} \tag{26}$$

where $I_v(x)$ is the intensity of the photon flux and is expressed in terms of energy/cm^2-s. Ideally, if 90 percent of the incident flux is to be absorbed in a distance d, then the flux emerging at $x = d$ will be 10 percent of the incident flux, and for CdTe $\alpha = 10^4$, then

$$d = (1/\alpha)ln(1/0.1) = (1/10^4)ln(10) = 2.30\ \mu m \tag{27}$$

As the incident photon energy increases, the absorption coefficient increases rapidly, so that the photon energy can be totally absorbed in a very narrow region.

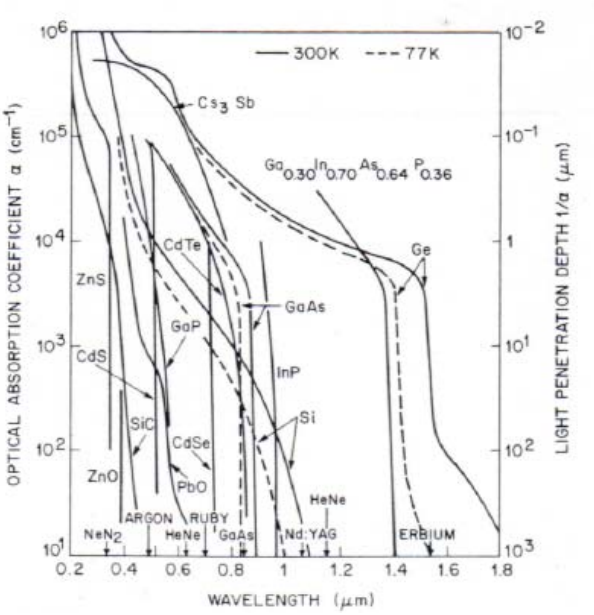


Figure 49. Optical absorption coefficients for various semiconductor materials, including CdTe. [27].

4.3.2 Experimental Details and Results

In this study, all thin CdS/CdTe solar cells were of the superstrate configuration. The device structure was Glass/SnO_2/CdS/CdTe/C:HgTe-Cu. The substrates were Corning 7059 borosilicate glass. Before device fabrication, substrates were cleaned in a dilute hydrofluoric acid (HF) solution for approximately 10 seconds, followed by a deionized (DI) water rinse. The front contact structure consists of a SnO_2 bi-layer (low-ρ/high-ρ), deposited by chemical vapor deposition (CVD); the thickness and sheet resistance of the bi-layer were approximately 1 μm and 7-8 Ω/□ respectively [7]. The CdS films were deposited using the chemical bath deposition (CBD) process in an

aqueous bath at 85°C to a thickness of approximately 0.1 μm. The CdTe films were deposited by close-spaced sublimation (CSS) at substrate temperature and source temperature of 500°C and 630°C respectively. Following the CdTe deposition, the device structure was subjected to a heat treatment in the presence of $CdCl_2$ onto the CdTe surface by evaporation, and subsequently heat treating the structures at 390°C at atmospheric pressure in the presence of O_2 for 15 minutes. The back contact process consisted of a cleaning step, where the CdTe surface was etched using 0.1 % by volume Br_2/methanol solution for 10 seconds, followed by the application of a graphite paste doped with HgTe:Cu [38, 77] and a heat treatment in inert ambient at 400°C. After formation of the back contact, indium was soldered around the cell areas to serve as a front electrode. Solar cells were characterized using standard solar cell techniques, such as dark and light J-V, and spectral response (SR) measurements.

Recent focus in CdTe solar cell research is being dedicated to improving solar cell efficiencies and reducing production cost by minimizing materials requirements with the utilization of ultra-thin film CdTe devices. Considering the typical state-of-the-art performance characteristics of 840–850 mV, 74–76 %, and 24–26 mA/cm^2, for open-circuit voltage (V_{OC}), fill factor (FF), and short-circuit current density (J_{SC}) respectively [7], one approach to advance efficiencies and reduce cost is by using ultra-thin layers of CdTe, and scaled down deposition process conditions. This section describes the results of optimizing the CdTe thickness for maximum absorption in the long range wavelength, and of optimizing the corresponding scaled down deposition process conditions. The two main post-deposition processes ($CdCl_2$ treatment and back contact diffusion) require reoptimization for thin CdTe structures [78]. A. Compaan showed in Ref. [79] from high

angle X-ray diffraction (XRD) that chloride processing produces the usual intermixed alloy layer of CdSTe more quickly in the cells with thin CdTe. The use of their standard 30 minute $CdCl_2$ treatment at 387°C resulted in a thicker alloyed layer that was detrimental to cell performance [78]. They found the optimum treatment time in their process of RF sputtering of CdTe and CdS at approximately 260°C to be approximately 10 minutes. In our process of deposition of CdTe by CSS, and CdS by CBD, our treatment time was 15 minutes at 390°C. We have not reoptimized this process for our thin CdTe structures. Figure 50 illustrates that the transmission increases, with decreasing CdTe thickness. However, the sharpness of the CdTe absorption edge deteriorates significantly at CdTe thicknesses below 0.8 μm, negatively affecting the overall device performance and solar cell efficiency.

Figure 51 shows the light *J-V* characteristics of the ultra thin CdTe/CdS cells fabricated. The slope of the *J-V* characteristics at reverse bias, which is used as an approximation of the shunt resistance (R_{SH}), appears to be equivalent and infinite for the last four devices. However, there is a significance difference in the behavior of the curves around V_{OC}. All of the devices exhibit a series resistance (R_S), which appears to increase for the thinner CdTe devices (0.8 – 1.0 μm).

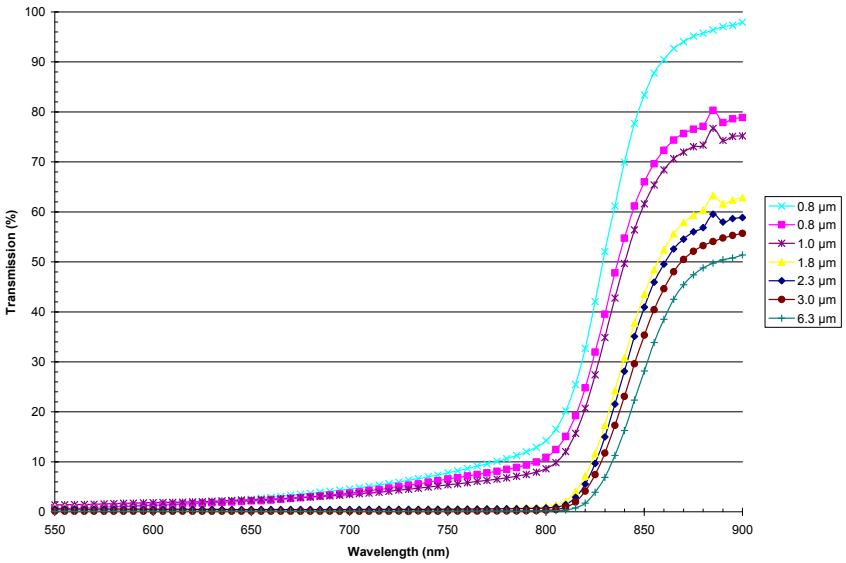


Figure 50. Transmission of solar cells with varied CdTe thicknesses ranging from 0.8 µm to 6.3 µm.

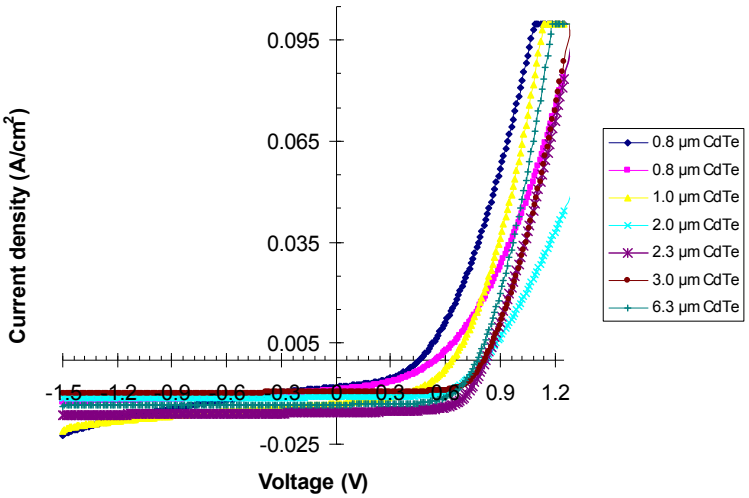


Figure 51. Light *J-V* characteristics for ultra thin CdTe solar cells, with varied CdTe thicknesses ranging from 0.8 µm to 6.3 µm.

Figure 52 shows the spectral response (SR) characteristics of the solar cells. The SR in the blue region (400 – 500 nm) was in the 30 – 35% range for the last four devices, indicating that the CdS thickness was appropriate to allow a major portion of the light above its band gap to reach the ultra thin CdTe. The three devices with the thinnest layers of CdTe exhibited significant recombination losses that further deteriorated in 600 – 800 nm wavelengths.

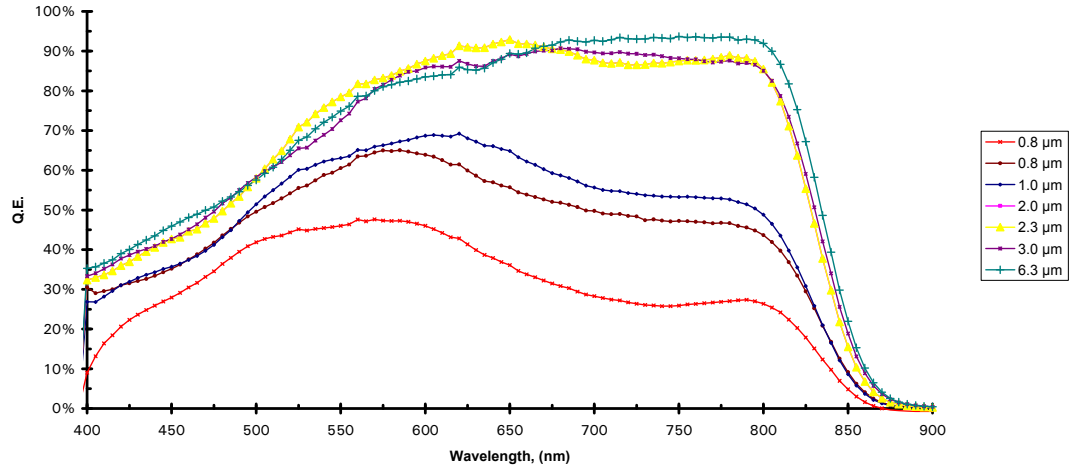


Figure 52. Spectral response characteristics for ultra thin CdTe solar cells. Thinner CdTe cells exhibit significant recombination losses, especially in the long wavelengths.

Table 6 summarizes the solar cell characteristics for the varied CdTe thicknesses ranging from 0.8 – 6.3 µm. Cells below the line all exhibit efficiencies greater than 11%, with CdTe thickness ranging from 2.0 – 6.3 µm. Cells above the line exhibit low efficiencies, because of the thinness of CdTe, which resulted in significant recombination

losses, shown in Figure 52. The best cell efficiency was 12.2%, with a CdTe thickness of 3.0 μm, 820 mV V_{OC}, 70% FF, and 21.30 mA/cm^2 J_{SC} based on the SR measurement.

Table 6. Summary of solar cell performance based on different CdTe thickness ranging from 0.8-6.3 μm.

Thickness (μm)	Sample ID	Voc (mV)	Jsc(mA/cm^2)	FF (%)	η (%)
0.8	3-14-1A	460	9.49	44	1.9
0.8	3-07-1D	550	14.04	41	3.2
1.0	3-07-1B	640	15.22	47	4.6
2.0	3-07-1A	820	21.45	64	11.3
2.3	3-07-1C	820	21.45	67	11.8
3.0	**3-14-1B**	**820**	**21.30**	**70**	**12.2**
6.3	3-14-1C	770	21.98	66	11.2

4.3.3 Conclusions

Ultra thin superstrate and substrate CdTe solar cells were fabricated and analyzed. The best cell efficiency was 12.2% superstrate cell, with a CdTe thickness of 3.0 μm, 820 mV V_{OC}, 70% FF, and 21.30 mA/cm^2 J_{SC} based on the SR measurement. At 2.0 μm CdTe, a cell with 11.3% efficiency was fabricated. Further work is required in the evaluation range of thicknesses, including the 2.3 μm optimum thickness of CdTe that will absorb 90% of the incident photon energy. Also, additional work is required in the optimization of scaling down deposition process conditions, to maximize device performance and efficiency.

4.4 Development of a Barrier Layer

4.4.1 Introduction

Thin stainless steel (SS) foils are used as the substrate for the development of CdTe solar cells because of its material properties, high temperature stability, commercial availability and cost. A potential problem with the use of a stainless steel foil as the substrate is the diffusion of iron (Fe), chromium (Cr) and other elemental impurities into the layers of the solar cell device structure during high temperature processing. A diffusion barrier limiting the out diffusion of these substrate elements is being investigated in this study. Silicon nitride (Si_3N_4) films deposited on SS foils are being investigated as the barrier layer, to reduce or inhibit the diffusion of substrate impurities into the solar cell. Si_3N_4 coefficient of thermal expansion (CTE) of $3.2x10^{-6}$/°K is close to both the back contact layer Molybdenum, with a CTE of $5.1x10^{-6}$/°K and the absorber CdTe, with a CTE of $5.9x10^{-6}$/°K, minimizing thermal expansion mismatch in the device. It has already been shown by others, that substrate impurities like Fe and Cr in the cell's absorber can lead to reduced cell efficiencies [15, 80]. In this study, the effect of the Si_3N_4 barrier layer is being evaluated for its effect on cell efficiency and overall device performance. The optimum Si_3N_4 barrier thickness is also being determined.

4.4.2 Experimental Details and Results

All thin CdTe/CdS solar cells discussed in this paper are of the substrate configuration shown in Figure 43. The substrates were flexible stainless steel foil, and prior to solar cell fabrication were ultrasonically solvent-cleaned in successive rinses of acetone, methanol and deionized water. The baseline metallization electrode structure consisted of a molybdenum (Mo) bi-layer, deposited by rf-sputtering at room temperature; the thickness of the Mo bi-layer was approximately 0.5 μm. The Si_3N_4 layer was deposited by rf sputtering at room temperature and at 300°C to relieve the stress in the thicker Si_3N_4 films; the thickness of the Si_3N_4 ranged from 0.05-1.0 μm. Both the CdTe and CdS layers were deposited by CSS at substrate temperatures in the 400-650°C range; the CdTe and CdS films were in some instances deposited in-situ. The solar cell structures were heat treated in the presence of $CdCl_2$ in O_2-containing ambient. The baseline transparent front contact consisted of ITO deposited by rf-sputtering at temperatures in the range of 200-300°C, and a thickness of 0.2-0.3 μm. Solar cells were characterized using standard solar cell techniques such as dark and light J-V, and spectral response (SR) measurements. SIMS, EDS, SEM and XRD measurements were performed to study the structure and morphology of the films and devices.

4.4.2.1 Diffusion of Substrate Impurities

The diffusion of iron (Fe), chromium (Cr) and other substrate elements into the CdTe layer during high temperature processing was investigated by Secondary Ion Mass

Spectrometry (SIMS) and EDS lines measurements. It has been reported in literature that during the deposition of CIGS on steel foils, detrimental impurities like Fe diffuse from the substrate, negatively affect device performance, and deteriorate the cell's efficiency [15, 80-82]. Figure 53 shows a SIMS depth profile of out-diffused substrate impurities Fe and Cr measured on a thin film CdTe solar cell fabricated on a stainless steel substrate without a diffusion barrier layer. SIMS analysis was conducted at the National Renewable Energy Laboratory (NREL). The structure of the sample #3-2-2A in Figure 53 is SS/Mo bi-layer/ZnTe/CdTe/CdS/SnO_2/ITO. This sample has no diffusion barrier. The results show a high concentration of out diffused substrate impurity Fe in the absorber layer CdTe. Figure 54 shows an EDS lines measurement of sample #3-2-2A, also showing out diffused Fe and Cr impurities from the substrate into the absorber CdTe layer. The diffusion of Fe could be strongly reduced by a diffusion barrier layer. Figure 55 is the corresponding SEM cross section image showing the location of the EDS lines measurement.

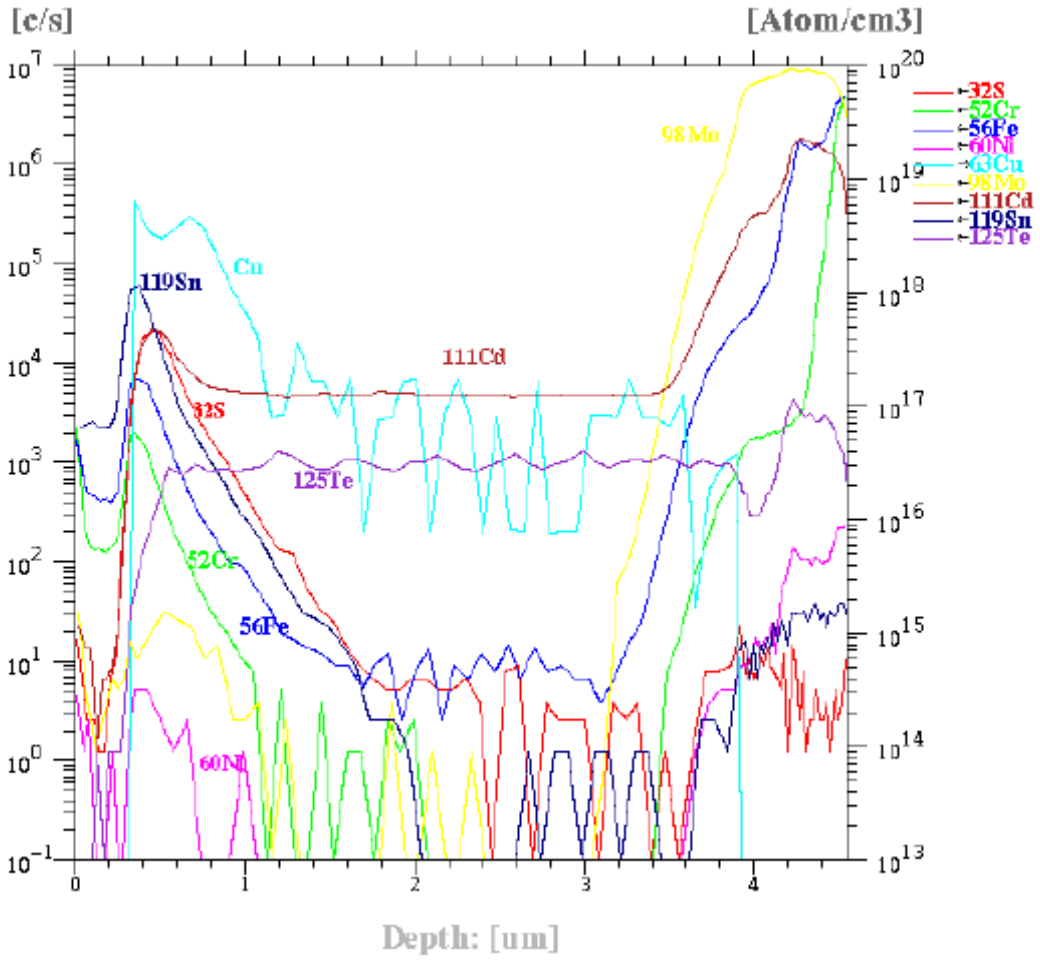


Figure 53. SIMS depth profiles showing high concentrations of out-diffused substrate impurities Fe and Cr measured on a thin film CdTe solar cell fabricated on a stainless steel substrate without a diffusion barrier layer.

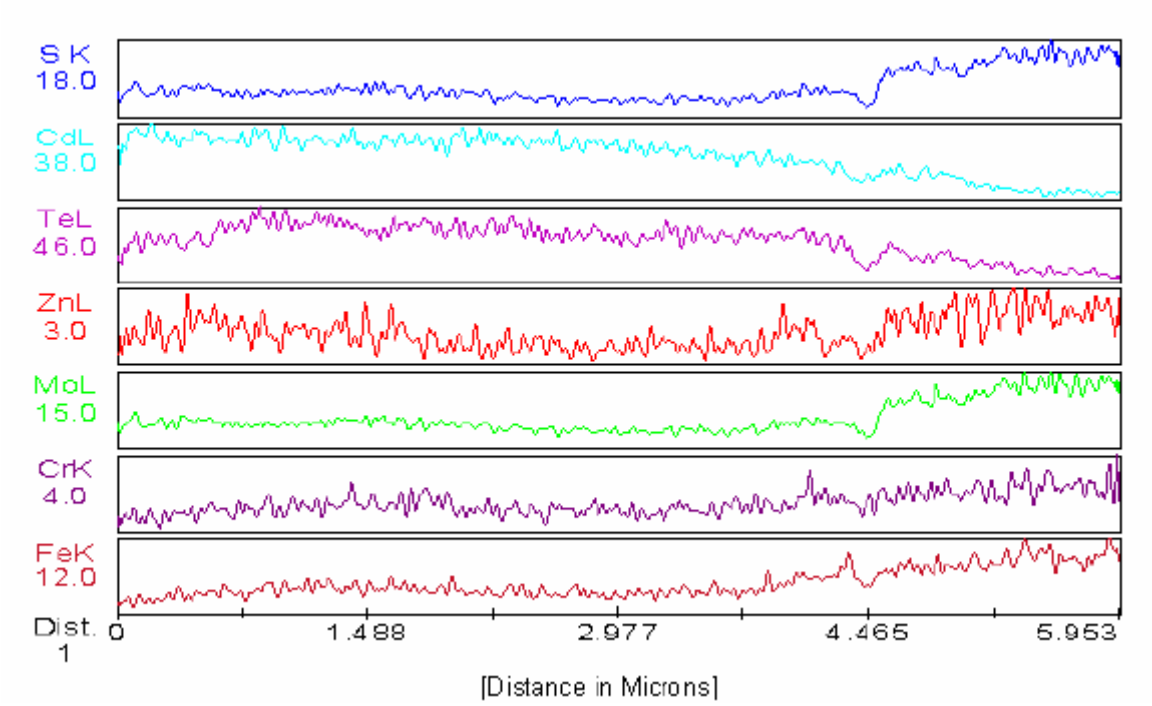


Figure 54. EDS lines measurement of sample #3-2-2A also showing out diffused Fe and Cr impurities from the substrate into the absorber CdTe layer.

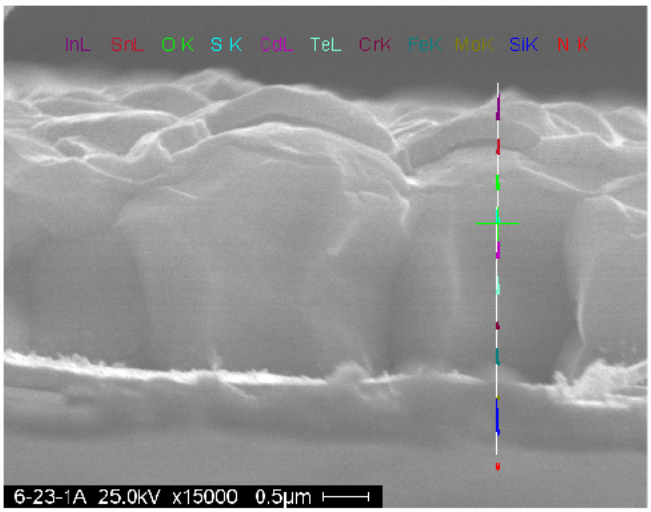


Figure 55. SEM cross section image corresponding to the EDS lines measurement performed in Figure 54, showing the location of the high concentration of Fe in CdTe.

4.4.2.2 Diffusion Barrier

Various diffusion barriers are capable with respect to their effectiveness in blocking substrate constituent diffusion into the CdTe absorber. Barriers include Si_3N_4, SiO_2, Al_2O_3, Cr and thicker metallization Mo layers. This study focuses on Si_3N_4 layers deposited onto steel foils at varying thicknesses and temperatures. The diffusion of Fe and Cr into CdTe was measured.

The structure of the sample #6-23-1A in Figure 57 is SS/Si_3N_4/Mo bi-layer/ZnTe/CdTe/CdS/SnO_2/ITO. This sample has a 0.5 μm diffusion barrier. The results show a very low concentration of out diffused substrate impurity Fe in the absorber layer CdTe. This figure shows the EDS lines measurement showing a significant reduction in out diffused Fe and Cr impurities from the substrate into the absorber CdTe layer.

In ref. [15], CIGS thin film solar cells were fabricated on steel substrates with and without a diffusion barrier layer. The results indicate all cell parameters are higher for cells prepared on steel sheet substrates with diffusion barriers than for cells on bare steel substrates without barriers, as shown in the *JV* comparison curves in Figure 56 [15].

Initial data in this study show increased cell performance and efficiency in devices with a diffusion barrier, as illustrated in Table 7. Currently, Si_3N_4 is being studied as a barrier layer. Further studies are required to evaluate other barrier layers.

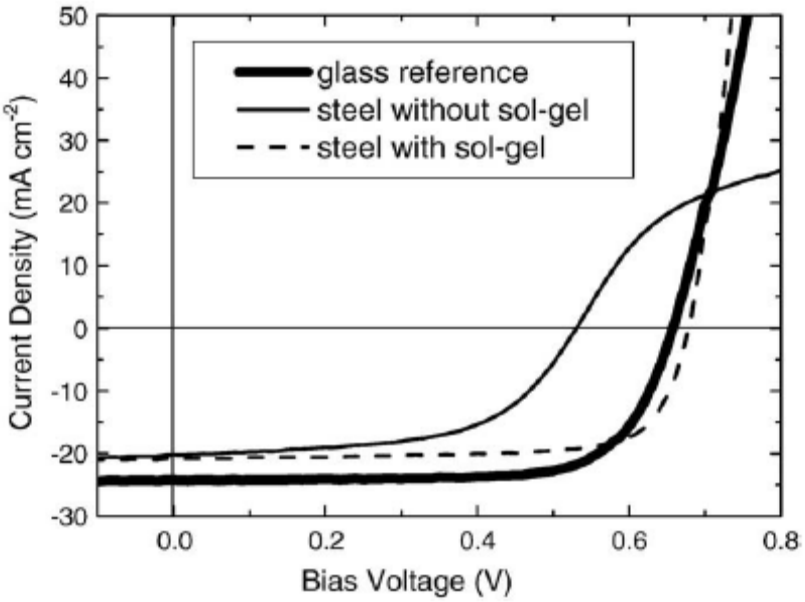


Figure 56. *JV* characteristics of CIGS solar cells with and without a diffusion barrier layer. [15]

Table 7. Results of solar cells fabricated with and without a Si_3N_4 barrier layer. The device fabricated with a barrier shows an increase in cell efficiency.

Sample Number	**Si_3N_4 t (Å)**	**Device Layers**	**V_{OC} (mV)**	**FF (%)**
3-2-2A	0	SS/Mo/ZnTe/CdTe/CdS/SnO_2/ITO	590	22
7-6-3B	500	SS/Si_3N_4/Mo/ZnTe/CdTe/CdS/SnO_2/ITO	620	33

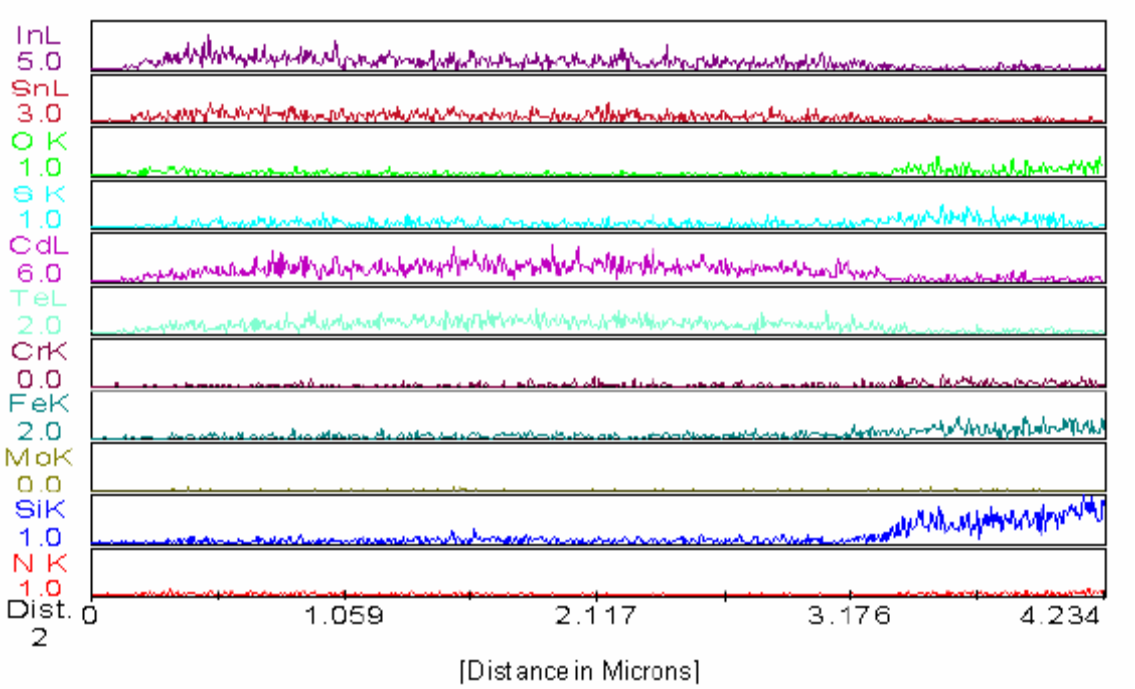


Figure 57. EDS lines measurement of sample #6-23-1A with a 0.5 µm Si_3N_4 barrier, showing a significant reduction in out diffused Fe and Cr impurities from the substrate into the absorber CdTe layer.

4.4.2.3 Optimum Barrier Thickness

In the work of D. Herrmann et al. in their *High-Performance Barrier Layers for Flexible CIGS Thin-Film Solar Cells on Metal Foils* [83], electrical defects and their sources in the SiO_x barrier layer were identified. Main defects were caused by mechanical damages (scratches, scoring and rolling traces) of the substrate. Surface roughness, metallic particles and larger fragments were also sources of electrical defects in the barrier layer. With the help of substrate pre-treatment and the deposition of sufficiently

thick SiO_x layers, perfect insulation properties could be achieved [83]. This is shown in Figure 58 for SiO_x films of 1, 2 and 3 µm thickness on Kovar® substrates, where the 3 µm film showed perfect insulation properties [83].

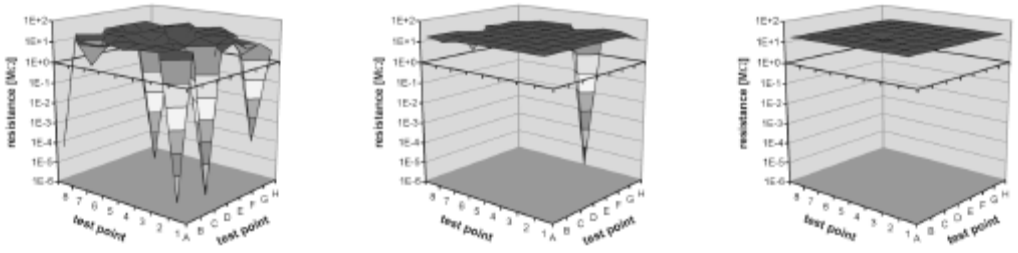


Figure 58. Insulation of (left to right) 1, 2 and 3 µm thick SiO_x layers on Kovar® foils. [83]

Initial data in this study show increased cell performance and efficiency in devices with a thicker diffusion barrier, as illustrated in Table 8. This study is ongoing to determine the optimum Si_3N_4 barrier thickness and deposition conditions for thin film CdTe solar cells deposited on flexible stainless steel substrates.

Table 8. Initial results of solar cells with different Si_3N_4 barrier thicknesses.

Sample Number	Si_3N_4 t (Å)	Device Layers	V_{OC} (mV)	FF (%)
6-17-2A	2,500	SS/Si_3N_4/Mo/CdTe/CdS/SnO_2/ITO	100	26
6-23-1A	5,000	SS/Si_3N_4/Mo/CdTe/CdS/SnO_2/ITO	370	40

4.4.2.4 Substrate Type and Surface Roughness

Substrate roughness is a factor that also effects film growth and microstructure prepared on flexible metal substrates, and subsequent solar cell device performance and efficiency. In a study by W. Batchelor et al. [81] examining the effect of substrate roughness on device performance, CIGS cells were prepared on commercially available foils with different surface roughness and finishes. The results shown in Table 9 indicate that there is a correlation between RMS substrate surface roughness and subsequent device performance. Solar cell performance increased with a decrease in substrate surface roughness. In a study by R. Wuerz et al. [15], properties of steel substrates and their effect on device performance were also investigated. The results are shown in Table 10 and also show that solar cell device performance increased with a decrease in substrate surface roughness. It was shown that a polished surface makes an ideal layer growth possible [83]. D. Herrmann et al. in their study of CIGS solar cells on metal foils [83] evaluated CIGS solar cells on three different types of metal substrates as shown in Table

11. The results indicate that the best values were obtained on titanium, but on stainless steel and Kovar® efficiencies were only lower by about 1%. This was due to slight decreases in fill factors and reduced open-circuit voltages.

Table 9. Average surface roughness and corresponding CIGS device parameters. [81]

Steel Type	Surface Finish	RMS roughness [Å]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
A	#2	571	606 593	25.27 26.54	57.6 65.5	8.82 10.3
A	#2 Bright	664	527 437	20.83 25.51	58.4 54.7	6.4 6.10
A	Bright	865	528 436	17.57 24.14	57.4 54.8	5.33 5.76

Table 10. Average surface roughness and corresponding CIGS device performance. [15]

Substrate	D [μm]	Roughness R_a [nm]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
Cr steel 24	127	24	648	19.4	71	8.9
Cr steel 41	100	41	620	16.8	68	7.1

Table 11. CIGS solar cells on various substrates. [83]

CIGS solar cell	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	η [%]
on stainless steel	628	27.1	72	12.3
on Kovar®	608	27.8	72	12.2
on titanium	656	26.9	74	13.1

Substrate roughness strongly influences growth, crystal orientation and other properties of subsequent layers. Grain boundaries, defects, pinholes, gain size, orientation and packing density directly impact the overall solar cell device performance. CdTe solar cell devices were fabricated on five different substrates with different surface roughness, listed in Table 12. The effect of surface roughness on CdTe devices have not been performed yet. However, the substrate effect on grain morphology is shown in Figure 59. Results indicate that CdTe grains grow very differently on the different substrates due to the effects of the substrate microstructure, surface effects and mechanical properties of the substrate. There appears to be an inverse correlation between surface roughness and grain size, but more research is required in this area.

Table 12. Surface roughness and other properties of foils researched in this study.

Substrate Material	CTE (x 10^{-6}/°K)	ΔCTE (x 10^{-6}/°K)	Roughness RA (nm)	Lattice Parameter (Å)/Crystal
SS 316	16.5	10.6	19	3.5920/Cubic
SS 430	10.5	4.6	3	2.8839/Cubic
Ta	6.48	0.58	23	3.3058/Cubic
Mo	5.04	- 0.86	10	3.1472/Cubic
W	4.5	- 1.4	6	3.1648/Cubic

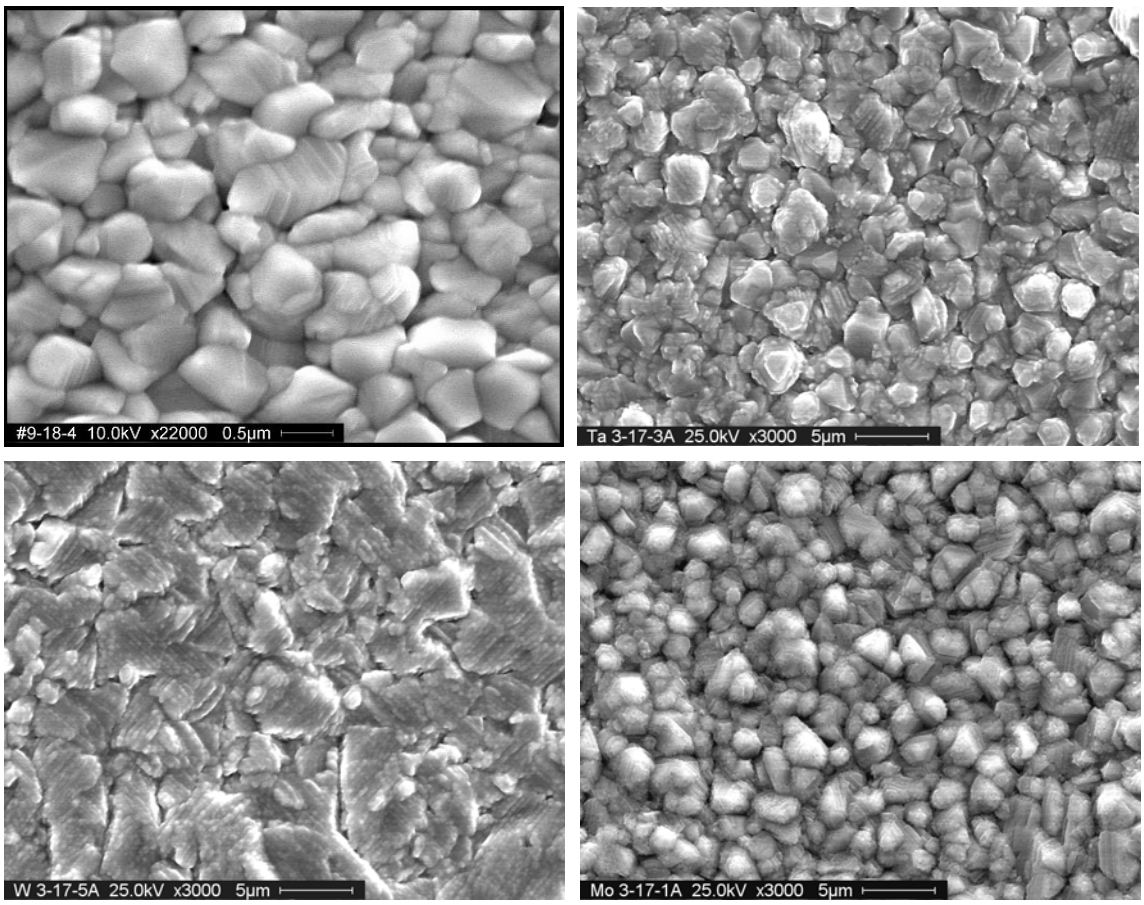


Figure 59. SEM images showing substrate effect on CdTe morphology on four different substrate foils. Top-left image is stainless steel foil, with grain sizes of 0.5-1.5 µm; top-right image is tantalum foil, with grain sizes of 2-4 µm; bottom-left image is tungsten foil, with grain size of 4-6 µm; bottom-right image is molybdenum foil, with grain size of 2-4 µm.

4.4.3 Conclusions

Effects of substrate impurity out-diffusion and substrate roughness on CdTe device performance are being evaluated. The diffusion of substrate elements Fe and Cr is evident in solar devices fabricated without a diffusion barrier layer. Use of a Si_3N_4 diffusion barrier layer has been shown to suppress the out-diffusion of substrate impurity elements, and improve solar cell device performance and efficiency. Additional research is required to evaluate the different material options available as barriers, and to determine their optimum thickness for best CdTe solar cell device performance. A preliminary inverse correlation can be seen between substrate roughness and CdTe device performance where smaller surface roughness values yield solar cell devices with higher efficiencies. A thicker Mo layer or a thicker barrier layer may serve as a smoothing or leveling layer. Additional research is required in this area to determine both the optimum substrate roughness and the best type of substrate foil that yield optimum CdTe solar cell device performance.

4.5 Flexible CdTe Solar Cells: 6.2% Efficiency

4.5.1 Introduction

Conventional polycrystalline thin film solar cells are usually manufactured on thick glass substrates and offer no weight advantage or shape adaptability for curved surfaces. Producing thin film solar cells on flexible metal foil substrates offers several

advantages for space as well as terrestrial applications. CdTe solar cells on glass substrates have efficiencies exceeding 16%, and recent development CdTe solar cells on flexible metal foils in a substrate configuration report efficiencies in the range of 3.8 to 8% [9, 11, 12]. Challenges in the development of CdTe devices on metallic substrates is the formation of an efficient ohmic contact with CdTe and the incorporation of an additional buffer layer as an ohmic contact to increase the cell efficiency. The criteria of matching thermal expansion coefficients and work function, limit the choice of substrate and contact materials. An additional consideration is the change to the ohmic contact properties, as a result of diffusion of impurities during the $CdCl_2$ annealing treatment and from the stainless steel substrate. Recent progress on the fabrication technology of CdTe/CdS solar cells on flexible metallic substrates is summarized in Table 13.

Table 13. Summary of flexible CdTe solar cells on metallic substrates.

Rank	Group	Efficiency
1	University of Toledo	7.8 %
2	University of South Florida	6.2 %
3	University of Kentucky and University of Texas	6.0 %
4	National Autonomous University of Mexico	3.5 %

4.5.2 Experimental Details and Results

Substrate type CdTe solar cells (see Figure 14) were fabricated on flexible 25.4 μm stainless steel foils. Prior to solar cell fabrication, substrates were ultrasonically solvent-cleaned in successive rinses of acetone, methanol and deionized water. The baseline metallization electrode structure consisted of a molybdenum (Mo) bi-layer, deposited by rf-sputtering at room temperature; the thickness of the Mo bi-layer was approximately 0.5 μm. Back contact buffer evaluated include: ZnTe by CSS in-situ with CdTe and CdS at substrate temperatures in the 400-650°C range, Sb_2Te_3 by thermal evaporation at substrate temperatures in the range of 200-300°C, Mo_2C by rf sputtering at substrate temperatures in the range of 200-300°C, and Au by thermal evaporation at room temperature. Both the CdTe and CdS layers were deposited by CSS at substrate temperatures in the 400-650°C range; the CdTe and CdS films were deposited in-situ. The solar cell structures were heat treated in the presence of $CdCl_2$ in O_2-containing ambient. The baseline transparent front contact consisted of ITO deposited by rf-sputtering at temperatures in the range of 200-300°C, and a thickness of 0.2-0.3 μm. Solar cells were characterized using standard solar cell techniques such as dark and light J-V, and spectral response (SR) measurements. SIMS, EDS, SEM and XRD measurements were performed to study the structure and morphology of the films and devices.

Results of five different categories of devices fabricated with different back contact buffer layers are summarized in Table 14. All of the devices fabricated were limited in device performance and efficiency directly as a result of the following:

1. As a result of the back contact materials used, all of the devices exhibit the presence of a back barrier that limits the solar cell V_{oc} and FF;
2. All of the devices were fabricated on stainless steel foil and are performance limited as a result of out-diffusion of impurities (Fe and Cr) from the stainless steel substrate;
3. All of the devices were significantly strained due to the large mismatch in the thermal expansion coefficient of the substrate and the CdTe absorber layer, and the ZnTe back contact buffer layer;
4. The surface roughness of the stainless steel substrate also limits the solar device performance and efficiency.

Even in the presence of all of the above device performance limitations, thin film CdTe solar cells were successfully fabricated on flexible stainless steel foil substrates with Mo as the metallization back contact layer. A typical device cross-sectional image is shown in Figure 60 for a cell with Mo/ZnTe back contact.

Table 14. Summary of devices fabricated with different back contact buffer layers.

Sample ID	Back Contact	Buffer Layer	Remaining Device Structure	V_{oc} [mV]	FF [%]	J_{sc} [mA/cm2]	η [%]
6-13-1B	Mo		CdTe/CdS/ITO	570	46	19.44	5.10
5-30-4B	Mo	ZnTe	CdTe/CdS/ITO	610	54	18.16	5.98
1-22-4A	Mo/ Mo_2C	Sb_2Te_3	CdTe/CdS/In_2O_3/ITO	580	51	19.42	5.74
1-11-2B	Mo	Mo_2C	CdTe/CdS/In_2O_3/ITO	630	48	18.27	5.52
6-26-1A	Mo	Au	CdTe/CdS/ITO	630	50	19.75	6.22

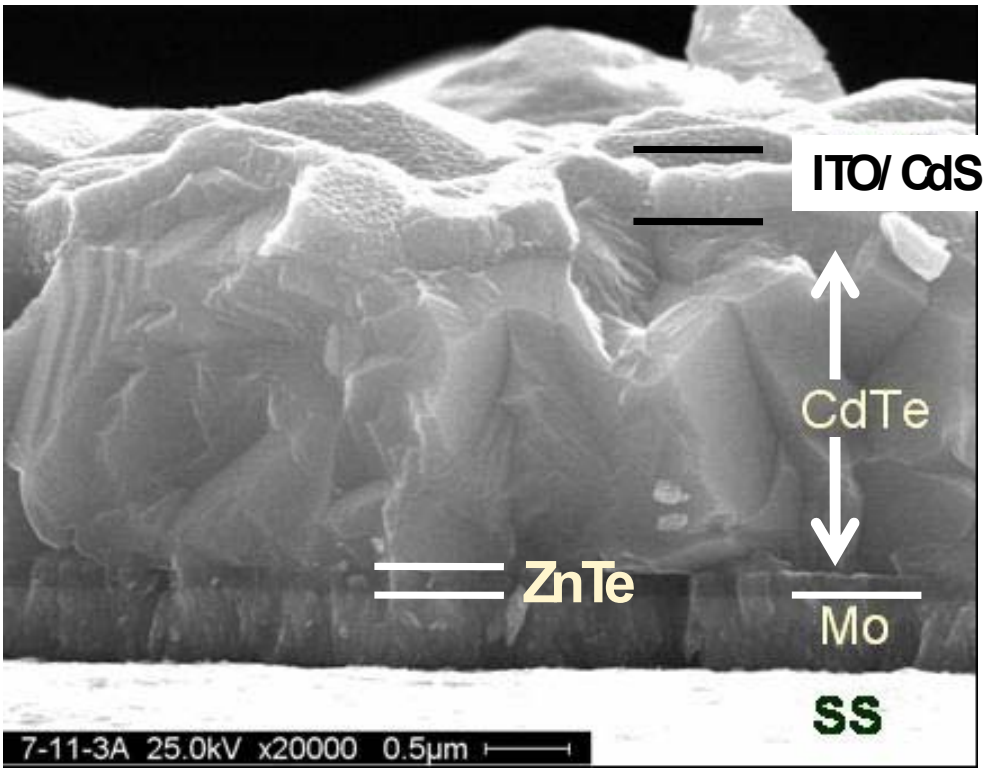


Figure 60. Cross section SEM image of foil/Mo/ZnTe/CdTe/CdS/ITO solar cell.

Devices fabricated with Sb_2Te_3 films prepared by evaporation of the Sb_2Te_3 compound exhibited better performance that appeared to improve with increasing deposition temperature (of the Sb_2Te_3 films). Cells contacted with Mo_2C exhibited promising performance. However, it should be noted that the solar cell fabrication process utilizing both contacts is not yet fully optimized and therefore trends may not hold true under an otherwise optimized process.

Cells contacted with ZnTe exhibited the best cost-effective performance to-date with efficiencies at the 6.0% level. Cells contacted with Au exhibited the best performance to-date with efficiencies exceeding the 6.0% level. Use of all the back contact buffer layers improved the cell's V_{OC}, FF and cell efficiency. Continued research is ongoing to identify a high work function material, which establishes an ohmic back contact with CdTe, without the back barrier effect. Figure 61 shows light I-V characteristics for substrate CdTe cells fabricated on foil substrates; the differences in I_{SC} are due to the cell's different areas; and J_{SC}'s calculated from SR data yield currents in the 20-22 mA/cm^2 range. Figure 62 shows a SR comparison of CdTe solar cells fabricated with the different back contact buffer layers.

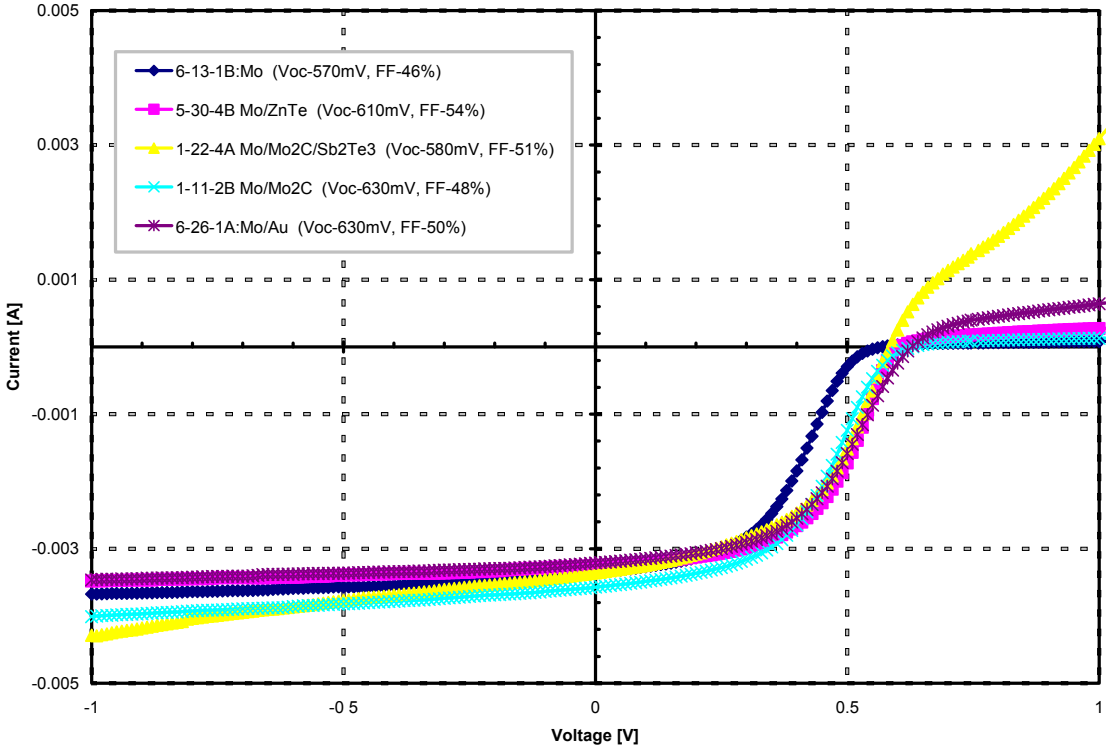


Figure 61. Light I-V for substrate CdTe cells fabricated on foil substrates. The differences in I_{SC} are due to the cell's different areas; J_{SC}'s calculated from SR data yield currents in the 20-22 mA/cm^2 range.

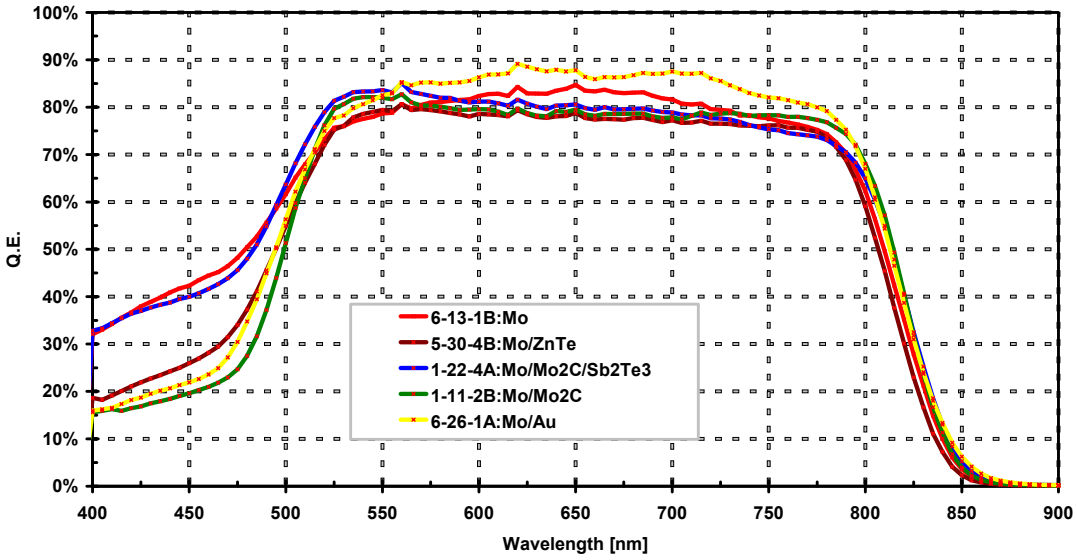


Figure 62. SR comparison of CdTe solar cells fabricated with different back contact buffer layers.

4.5.3 Conclusions

Solar cell results suggest that ZnTe is more suitable as a back contact material based on the highest V_{OC} obtained from ZnTe-contacted cells, even though this material was not intentionally doped (and exhibited high resistivity). This suggests that doping of ZnTe can result in significant improvements in the back contact characteristics and overall solar cell performance. All solar cells exhibited I-V characteristics with a significant roll-over in the 1st quadrant suggesting the presence of a strong barrier at the back contact as shown in Figure 61. Research is ongoing in the investigation of other high work function metals (Ir and Pt), suitable as potential back contact materials to substrate CdTe solar cells. Also, research is ongoing to develop a suitable diffusion

barrier to suppress out-diffusion of substrate impurities. Increases in solar cell device performance should be realized after the aforementioned enhancements are implemented. Substrate CdTe solar cells fabricated on flexible foil have to-date exceeded efficiencies of 6%.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

Challenges in the development of CdTe solar cells on metallic substrates include the formation of an efficient ohmic back contact to CdTe or the incorporation of an additional buffer layer as a pseudo-ohmic contact, to increase the solar cell's overall performance and efficiency. Also, the criteria of matching thermal expansion coefficients and work function, limit the choice of substrate and contact materials. An additional consideration is the change to the ohmic contact properties, as a result of diffusion of impurities during the $CdCl_2$ annealing treatment and also out-diffusion of impurities from the stainless steel substrate during the high temperature processing of the solar cell. Many of these challenges were investigated in this research, the results presented and conclusions follows.

Mismatch minimization of the substrate's CTE promotes adhesion and device performance of the CdTe solar cell device onto the flexible foil substrate (for as-deposited films). The effect of the $CdCl_2$ chemical treatment on the CdTe solar cell device increases flaking and delamination. Mo bi-layers reduce surface roughness and promote adhesion. Adhesion has significantly improved and studies continue with

minimizing CTE mismatch in the foil substrate, minimizing the surface roughness and optimizing the $CdCl_2$ treatment to promote adhesion of substrate CdTe thin film solar cells deposited on flexible foil substrates.

Different materials were investigated as back contact candidates for substrate CdTe thin film solar cells deposited on flexible foil substrates: Mo, ZnTe, Sb_2Te_3, Mo_2C and Au. The Sb_2Te_3 resistivity was found to decrease with deposition temperature; the resistivity for films studied to date was found to be in the range $8.0x10^{-6}$ - $5.4x10^{-5}$ Ω·m. The decrease in resistivity of Sb_2Te_3 is attributed to an increase in carrier mobility. Solar cell results suggest that ZnTe is more suitable as a back contact material based on the highest V_{OC} obtained from ZnTe-contacted cells, even though this material was not intentionally doped (and exhibited high resistivity). This suggests that doping of ZnTe can result in significant improvements in the back contact characteristics and overall solar cell performance.

Cells contacted with ZnTe exhibited the best cost-effective performance to-date with efficiencies at the 6.0% level. Cells contacted with Au exhibited the best performance to-date with efficiencies exceeding the 6.0% level. Use of all the back contact buffer layers improved the cell's V_{OC}, FF and cell efficiency. All solar cells exhibited I-V characteristics with a significant roll-over in the 1st quadrant suggesting the presence of a strong barrier at the back contact. Substrate CdTe solar cells fabricated on flexible foil have to-date reached efficiencies of 6%.

5.2 Future Work

Future work should address the following areas:

1. Ohmic back contacts:
    a. ZnTe doping,
    b. further studies of the properties of Sb_2Te_3 as a function of deposition parameters,
    c. use of high work function metals, Ir and Pt as back contacts,
    d. optimization of the solar cell process for each type of contact material.
2. Continued studies of thermal expansion coefficient mismatch minimization, by
    a. incorporation of a stress-relief anneal after CdTe deposition
    b. fabricating devices on Ta foil as a substrate, and using a substrate diffusion barrier layer.
3. Developing a diffusion barrier layer to suppress out-diffusion of impurities from the metallic substrate during high temperature processing by
    a. evaluating barrier materials: Si_3N_4, SiO_2, Al_2O_3, Mo and Cr
    b. optimizing barrier thickness.
5. Utilizing the 'Stress-induced lift-off method' (SLIM-Cut) process, illustrated in Figure 63, to fabricate thin film CdTe on flexible metallic substrates, lifting off the entire device including a deposited metallic substrate layer. In the SLIM-Cut process [84], a high thermal stress is induced by a metallization layer, resulting in the release of a thick metal foil.

Addressing the above listed items is believed to significantly increase the V_{OC} and FF of thin film CdTe solar cells on flexible metallic substrates.

Figure 63. 'Stress-induced lift-off method' (SLIM-Cut) process. A high thermal stress is induced by a metallization layer, resulting in the release of a 50 µm Si foil. The top row shows the remaining substrate and the bottom row, the thin lifted-off silicon layer. [84]

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